Mini LFR - Bitstream Generation Procedure

1 Generates scripts files

Clean the project directory, and run the makefile scripts command to generate all project's files.

```
# clean the project and re-generates the scripts
$> make distclean scripts
```

The files MINI_LFR_top_libero.prj should be created.

2 Launch Libero IDE

Open the project MINI_LFR_top_libero.prj with Libero IDE v9.1.
Capture1.PNG

2.1 Synthesis

Synthesis tools should be configured to use **Synplify** version **2012-03A-SP1-2**.

Launch the synthesis step (You must not add constraint file).
In the synplify Pro windows, click on the Run button.

The project status obtained should be :

Capture2.PNG

> You must verfify the block RAM's usage. The expected value is 100.
>
> If it's around 60/70, LEON3 processor is not mapped. In this case, you must clean your project and restart the generation procedure.

You can close Synplify and return to Libero.

If the Sythesis step is green like that :

You must activate the option Detect new files on disk automatically in the project settings.

Capture3.PNG
Capture4.PNG

2.2 Place&Route

Launch the Place&Route step. You must add the constraint files :

- default.pdc (Input/Output constraint)
- MINI-LFR_PlaceAndRoute.sdc (Timing constraint)

Capture5.PNG

2.2.1 Compile Step

Capture6.PNG
Run the Compile step.

2.2.2 Layout Step

Capture7.PNG
Run the Layout step.

In the Layout options windows, select Advanced Layout Options :

Capture8.PNG
And checked those options :

Capture9.PNG
Click Ok and wait...

Capture10.PNG
2.2.3 Timing Analyser

Launch theTiming Analyser.

Capture11.PNG
2.2.3.a SpaceWire Output

You must verify the SpaceWire output timing for the Max and Min delay.

Capture12.PNG
Capture19.PNG
The ouput skew is equal to Ouput_SOut timing - Ouput_DOut timing. This output skew must be positive.

In this exemple,

SPW_NOM skew max = 13.907 - 15.882 = -1.975 ns

SPW_NOM skew min = 6.367 - 7.317 = -0.950 ns

SPW_RED skew max = 17.937 - 13.510 = 4.427 ns

SPW_RED skew min = 8.304 - 6.175 = 2.129 ns

The SPW_NOM interface must be modified. In ChipPlanner, we will move element in the SPW_NOM path to have a positive skew in min and max delay.
Capture13.PNG
Capture14.PNG

2.2.3.b SpaceWire Input

You must also verify the SpaceWire input timing. For that, you must add a new set for SPW_INPUT:

Capture15.PNG
and configure it like that :
you
Capture16.PNG

You obtain those timing for min and max delay.

Capture17.PNG
Capture18.PNG
You must also add a new set for the FF setup time :

Capture20.PNG
Capture21.PNG
In resume, for the input SPW_NOM interface :

```
        <tr>
        <th colspan=2> Signal Type </th>        <th> max delay</th> <th>min delay</th>
        </tr>
    </thead>
    <thead>
        <tr>
        <th colspan=4 align="center" bgcolor="#C0C0C0"> SPW_NOM_IN </th>
        </tr>
    </thead>
    <tbody>
        <tr>    <td rowspan=4>r_FF</td>     <td>Strobe to CLK</td>  <td>7.230 ns</td>   <td>3.497
ns</td>   </tr>
    <tr>                    <td>Data   to CLK</td>  <td>8.046 ns</td>   <td>3.807 ns</td>   </tr>
    <tr>                    <td>Data   to D  </td>  <td>1.700 ns</td>   <td>0.692 ns</td>   </tr>
    <tr>                    <td>D to Q  </td>   <td>0.888 ns</td>   <td>0.413 ns</td>   </tr>
```

```
    <tr>    <td rowspan=4>nr_FF</td>    <td>Strobe  to CLK</td> <td>7.315 ns</td>   <td>3.543 ns</
td>   </tr>
    <tr>                    <td>Data    to CLK</td> <td>8.131 ns</td>   <td>3.853 ns</td>   </tr>
    <tr>                    <td>Data    to D  </td> <td>1.767 ns</td>   <td>0.724 ns</td>   </tr>
    <tr>                    <td>D to Q  </td>   <td>0.888 ns</td>   <td>0.413 ns</td>   </tr>
    </tbody>
    <thead>
        <tr>
        <th colspan=4 align="center" bgcolor="#C0C0C0"> SPW_RED_IN </th>
        </tr>
    </thead>
    <tbody>
        <tr>    <td rowspan=4>r_FF</td>     <td>Strobe to CLK</td>  <td>11.601 ns</td>  <td>6.217
ns</td>   </tr>
    <tr>                    <td>Data   to CLK</td>  <td>12.845 ns</td>  <td>5.488 ns</td>   </tr>
    <tr>                    <td>Data   to D  </td>  <td>2.799 ns</td>   <td>1.246 ns</td>   </tr>
    <tr>                    <td>D to Q  </td>   <td>0.888 ns</td>   <td>0.413 ns</td>   </tr>

    <tr>    <td rowspan=4>nr_FF</td>    <td>Strobe  to CLK</td> <td>11.628 ns</td>  <td>6.236 ns</
td>   </tr>
    <tr>                    <td>Data    to CLK</td> <td>12.872 ns</td>  <td>5.507 ns</td>   </tr>
    <tr>                    <td>Data    to D  </td> <td>2.798 ns</td>   <td>1.246 ns</td>   </tr>
    <tr>                    <td>D to Q  </td>   <td>0.888 ns</td>   <td>0.413 ns</td>   </tr>
    </tbody>
```

The input skew is equal to : min(Time from strobe to CLK; Time from data to CLK) - Time Data to FF - FF Setup Time. This input skew must be positive.

```
        <tr>
        <th> skew </th>         <th colspan=2>max delay</th>    <th colspan=2>min delay</th>
        </tr>
    </thead>
    <thead>
        <tr>
        <th colspan=5 align="center" bgcolor="#C0C0C0"> SPW_NOM_IN </th>
        </tr>
    </thead>
    <tbody>
        <tr>    <td>skew r_FF</td>  <td>4.642 ns</td>   <td bgcolor="#00FF00">OK</td>   <td>2.392
ns</td>   <td bgcolor="#00FF00">OK</td>   </tr>
        <tr>    <td>skew nr_FF</td>     <td>4.660 ns</td>   <td bgcolor="#00FF00">OK</td>   <td>2.
406 ns</td>   <td bgcolor="#00FF00">OK</td>   </tr>
    </tbody>
    <thead>
        <tr>
        <th colspan=5 align="center" bgcolor="#C0C0C0"> SPW_RED_IN </th>
        </tr>
    </thead>
    <tbody>
        <tr>    <td>skew r_FF</td>  <td>7.914 ns</td>   <td bgcolor="#00FF00">OK</td>   <td>3.829
ns</td>   <td bgcolor="#00FF00">OK</td>   </tr>
        <tr>    <td>skew nr_FF</td>     <td>7.942 ns</td>   <td bgcolor="#00FF00">OK</td>   <td>3.
848 ns</td>   <td bgcolor="#00FF00">OK</td>   </tr>
    </tbody>
```

In our case, all SPW input skew are positive.
If MIN or MAX skew delay are not positive, you must launch the ChipPlanner tool to move r_FF and nr_FF closest to the CLK source and move XOR gate far away from input pads (SIN, DIN), nrFF:D and r_FF:D.

You can close the Timing Analyser.

2.2.4 Chip Planner

Launch ChipPlanner to move element in the netlist and try to fit the timing requirements (skew delay for the SPW_NOM Output interface).

Capture22.PNG
In our case, we want to increase SPW_NOM\ output skew. For that, we must increase Ouput_SOut timing and reduce the Ouput_DOut timing.

To reduce the output dout delay, we will select the last FF before the SPW_NOM_OUTPUT :

Capture23.PNG
and move closest to the ouput PAD :

Capture24.PNG
To increase the output SOut delay, we will select the last FF before the SPW_NOM_OUTPUT :

Capture25.PNG
and move far away from the ouput PAD :

Capture26.PNG
Now, you can clicked on Commit and Check button and close ChipPlanner.

You must relaunch the Layout step with those selected options :

Capture27.PNG
And finally, checked the timing update with the Timing Analyser.

2.2 Bitstream generation

Click on the Programming File tool.

Capture28.PNG
It's done !

Files

Capture2.PNG	39.8 KB	01/12/2016	Jean-Christophe Pellion
Capture3.png	21.5 KB	01/12/2016	Jean-Christophe Pellion
Capture4.PNG	29.5 KB	01/12/2016	Jean-Christophe Pellion
Capture5.PNG	28.3 KB	01/12/2016	Jean-Christophe Pellion
Capture6.PNG	7.37 KB	01/12/2016	Jean-Christophe Pellion
Capture7.PNG	7.59 KB	01/12/2016	Jean-Christophe Pellion
Capture8.PNG	28.4 KB	01/12/2016	Jean-Christophe Pellion
Capture9.PNG	20.1 KB	01/12/2016	Jean-Christophe Pellion
Capture10.PNG	7.75 KB	01/12/2016	Jean-Christophe Pellion
Capture11.PNG	2.52 KB	01/12/2016	Jean-Christophe Pellion
Capture1.PNG	144 KB	01/12/2016	Jean-Christophe Pellion
Capture12.PNG	26.7 KB	01/12/2016	Jean-Christophe Pellion
Capture13.PNG	19 KB	01/12/2016	Jean-Christophe Pellion
Capture14.PNG	18.3 KB	01/12/2016	Jean-Christophe Pellion
Capture15.png	10.2 KB	01/12/2016	Jean-Christophe Pellion
Capture16.PNG	18.3 KB	01/12/2016	Jean-Christophe Pellion
Capture17.PNG	23 KB	01/12/2016	Jean-Christophe Pellion
Capture18.PNG	21.2 KB	01/12/2016	Jean-Christophe Pellion
Capture19.PNG	19.7 KB	01/12/2016	Jean-Christophe Pellion
Capture20.PNG	11.7 KB	01/12/2016	Jean-Christophe Pellion
Capture21.PNG	11.2 KB	01/12/2016	Jean-Christophe Pellion
Capture22.PNG	4.15 KB	01/12/2016	Jean-Christophe Pellion
Capture23.PNG	48.8 KB	01/12/2016	Jean-Christophe Pellion
Capture24.PNG	14.2 KB	01/12/2016	Jean-Christophe Pellion
Capture24.PNG	14.2 KB	02/12/2016	Jean-Christophe Pellion

Capture26.PNG	21.9 KB	02/12/2016	Jean-Christophe Pellion
Capture27.PNG	8.24 KB	02/12/2016	Jean-Christophe Pellion
Capture25.PNG	9.51 KB	02/12/2016	Jean-Christophe Pellion
Capture28.PNG	7.74 KB	02/12/2016	Jean-Christophe Pellion