

# VHDLlib - IP\_documentation - # 38

## h1. IP Documentation

---

### h2. Sample Type

#### [Sample Type](#)

```
TYPE Samples IS ARRAY(NATURAL RANGE <>) OF STD_LOGIC_VECTOR(15 DOWNT0 0);
```

```
SUBTYPE Samples24 IS STD_LOGIC_VECTOR(23 DOWNT0 0);  
SUBTYPE Samples16 IS STD_LOGIC_VECTOR(15 DOWNT0 0);  
SUBTYPE Samples14 IS STD_LOGIC_VECTOR(13 DOWNT0 0);  
SUBTYPE Samples12 IS STD_LOGIC_VECTOR(11 DOWNT0 0);  
SUBTYPE Samples10 IS STD_LOGIC_VECTOR( 9 DOWNT0 0);  
SUBTYPE Samples8 IS STD_LOGIC_VECTOR( 7 DOWNT0 0);
```

```
TYPE Samples24v IS ARRAY(NATURAL RANGE <>) OF Samples24;  
TYPE Samples16v IS ARRAY(NATURAL RANGE <>) OF Samples16;  
TYPE Samples14v IS ARRAY(NATURAL RANGE <>) OF Samples14;  
TYPE Samples12v IS ARRAY(NATURAL RANGE <>) OF Samples12;  
TYPE Samples10v IS ARRAY(NATURAL RANGE <>) OF Samples10;  
TYPE Samples8v IS ARRAY(NATURAL RANGE <>) OF Samples8;
```

---

### h2. General Purpose

### h3. Edge Detection

#### [Edge Detection](#)

EdgeDetection permit to detect the edge of the sin signal.

p=. !{width: 20%}edge\_detection.png!

```
COMPONENT lpp_edge_detection  
PORT (  
clk : IN STD_LOGIC;  
rstn : IN STD_LOGIC;  
sin : IN STD_LOGIC;  
sout : OUT STD_LOGIC);  
END COMPONENT;
```

Signal	Direction	Size	Function	Active
clk	input	1	clock domain 1	rising edge
rstn	input	1	reset	low
sin	input	1	signal in	
sout	output	1	signal out	

#### [Edge to level](#)

EdgeToLevel permit to transform the positive edge information into a level information.

p=. !{width: 20%}edge\_to\_level.png!

```
COMPONENT lpp_edge_to_level  
PORT (  
clk : IN STD_LOGIC;  
rstn : IN STD_LOGIC;  
sin : IN STD_LOGIC;  
sout : OUT STD_LOGIC);  
END COMPONENT;
```

Signal	Direction	Size	Function	Active
clk	input	1	clock domain 1	rising edge
rstn	input	1	reset	low
sin	input	1	signal in	
sout	output	1	signal out	

### h3. Synchronizer

#### [SYNC\\_FF](#)

Sync\_FF permit to synchronize a signal A in the clock domain clk. Normally, A signal should be the output of a FF clocked in an other domain. You shouldn't have "logic" between the 2 domain.

You can configure the number FF use to synchronize (NB\_FF\_OF\_SYNC). This number is depending of the MTBF(Mean Time Between Failure).

p=. !{width: 15%}SYNC\_FF.png!

```
COMPONENT SYNC_FF_LPP_JCP
GENERIC (
NB_FF_OF_SYNC : INTEGER);
PORT (
clk : IN STD_LOGIC;
rstn : IN STD_LOGIC;
A : IN STD_LOGIC;
A_sync : OUT STD_LOGIC);
END COMPONENT;
```

Parameter	Type	Size	Description	Default
NB_FF_OF_SYNC	Integer		Number of FF	2

Signal	Direction	Size	Function	Active
clk	input	1	clock	rising edge
rstn	input	1	reset	low
sin	input	1	signal in	
sout	output	1	signal synchronized	

#### [SYNC\\_VALID\\_BIT](#)

SYNC\_VALID\_BIT permit to synchronize a signal of validity from clock domain clk\_in to clock domain clk\_out. A validity bit is a signal set "high" only one cycle and zero others. To Synchronize this type of signal, a first stage detect the positive edge, a second synchronizes this signal, and a last transform the edge information to a validity bit.

You can configure the FF number of the second stage (NB\_FF\_OF\_SYNC).

p=. !{width: 20%}SYNC\_VALID\_BIT.png!

```
COMPONENT SYNC_VALID_BIT_LPP_JCP
GENERIC (
NB_FF_OF_SYNC : INTEGER);
PORT (
clk_in : IN STD_LOGIC;
clk_out : IN STD_LOGIC;
rstn : IN STD_LOGIC;
sin : IN STD_LOGIC;
sout : OUT STD_LOGIC);
END COMPONENT;
```

Parameter	Type	Size	Description	Default
NB_FF_OF_SYNC	Integer		Number of FF	2

Signal	Direction	Size	Function	Active
clk_in	input	1	clock domain 1	rising edge
clk_out	input	1	clock domain 1	rising edge
rstn	input	1	reset	low
sin	input	1	valid bit clocked in domain 1	
sout	output	1	valid bit clocked in domain 2	

## h2. SoC (System On Chip)

### [Leon3\\_SocLeon3\\_Soc](#)

Leon3\_SoC is an IP which integrate all the basic IP for using a Leon3 System. This System is configurable :

- activate the DSU, AHB uart, APB UART, IRQ manager and timer manager
- activate the FPU and select the type of IP using for (netlist or rtl)

You can connect easily external AMBA IP. For example, if you have only one Leon3 and you want to add an AHB Master My\_AHB\_MST. You set NB\_AHB\_MASTER to 1 and connect My\_AHB\_MST\_ahbmi signal to the input ahbi\_m\_ext and My\_AHB\_MST\_ahbmo to ahbo\_m\_ext(1).

```
|.Number|.NAME|.Enable Parameter|.Address|.IRQ|
|5=.AHB Master|
|0 to NCPU-1|leon3s|||
|NCPU+NB_AHBMAS-1|ahbuart|ENABLE_AHB_UART|||
|5.|
|5=.AHB Slave|
|0|mctrl|0x00000000| | |
|1|apbctrl|0x80000000|
|2|dsu3|ENABLE_DSU|0x90000000|0|
|5.|
|5=.APB Slave|
|0|mctrl|0x80000000| | |
|1|apbuart|ENABLE_APB_UART|0x80000100|2|
|2|irqmp|ENABLE_IRQMP|0x80000200|
|3|gptimer|ENABLE_GPT|0x80000300|8|
|4|ahbuart|ENABLE_APB_UART|0x80000400|
```

p=. !{width: 40%}leon3\_SoC.png!

COMPONENT leon3\_soc\_LPP\_JCP

GENERIC (

```
fabtech : INTEGER;
memtech : INTEGER;
padtech : INTEGER;
clktech : INTEGER;
disas : INTEGER;
dbguart : INTEGER;
pclow : INTEGER;
clk_freq : INTEGER;
NB_CPU : INTEGER;
ENABLE_FPU : INTEGER;
FPU_NETLIST : INTEGER;
ENABLE_DSU : INTEGER;
ENABLE_AHB_UART : INTEGER;
ENABLE_APB_UART : INTEGER;
ENABLE_IRQMP : INTEGER;
ENABLE_GPT : INTEGER;
NB_AHB_MASTER : INTEGER;
NB_AHB_SLAVE : INTEGER;
NB_APB_SLAVE : INTEGER);
```

PORT (

```
clk : IN STD_ULOGIC;
rstn : IN STD_ULOGIC;
errrn : OUT STD_ULOGIC;
ahbrxd : IN STD_ULOGIC;
ahbtxd : OUT STD_ULOGIC;
urxd1 : IN STD_ULOGIC;
utxd1 : OUT STD_ULOGIC;
address : OUT STD_LOGIC_VECTOR(19 DOWNTO 0);
data : INOUT STD_LOGIC_VECTOR(31 DOWNTO 0);
nSRAM_BE0 : OUT STD_LOGIC;
nSRAM_BE1 : OUT STD_LOGIC;
```

```

nSRAM_BE2 :OUT STD_LOGIC;
nSRAM_BE3 :OUT STD_LOGIC;
nSRAM_WE :OUT STD_LOGIC;
nSRAM_CE :OUT STD_LOGIC;
nSRAM_OE :OUT STD_LOGIC;
apbi_ext :OUT apb_slv_in_type;
apbo_ext :IN soc_apb_slv_out_vector(NB_APB_SLAVE-1+5 DOWNT0 5);
ahbi_s_ext :OUT ahb_slv_in_type;
ahbo_s_ext :IN soc_ahb_slv_out_vector(NB_AHB_SLAVE-1+3 DOWNT0 3);
ahbi_m_ext :OUT AHB_Mst_In_Type;
ahbo_m_ext :IN soc_ahb_mst_out_vector(NB_AHB_MASTER-1+NB_CPU DOWNT0 NB_CPU));
END COMPONENT;

```

.Parameter	.Type	.Size	.Description	.Default
fabtech	INTEGER		Target technologie	apa3e
memtech	INTEGER		Memory Target technologie	apa3e
padtech	INTEGER		Pad Target technologie	inferred
clktech	INTEGER		Clock target technologie	inferred
disas	INTEGER		Activate the disassembler	0
dbguart	INTEGER		Activate debug uart	0
pclow	INTEGER			2
clk_freq	INTEGER		Clock input frequency (in kHz)	25000
INB_CPU	INTEGER		Number of Leon3	1
ENABLE_FPU	INTEGER		Enable the FPU	1
FPU_NETLIST	INTEGER		Select the FPU Used (1=> NetList, 0=> RTL)	1
ENABLE_DSU	INTEGER		Enable the Debug System Unit	1
ENABLE_AHB_UART	INTEGER		Enable AHB UART	1
ENABLE_APB_UART	INTEGER		Enable APB UART	1
ENABLE_IRQMP	INTEGER		Enable irq manager	1
ENABLE_GPT	INTEGER		Enable the timer	1
INB_AHB_MASTER	INTEGER		Number of AHB Master outside the SoC	0
INB_AHB_SLAVE	INTEGER		Number of AHB Slave outside the SoC	0
INB_APB_SLAVE	INTEGER		Number of APB Slave outside the SoC	0

U5

.Signal	.Direction	.Size or Type	.Function	.Active
clk	input	1	clock	rising edge
rstn	input	1	reset	low
errorn	output	1	leon 3 error signal	
ahbrxd	input	1	AHB uart Rx Signal	
ahbtxd	output	1	AHB uart Tx Signal	
urxd1	input	1	APB uart Rx Signal	
utxd1	output	1	APB uart Tx Signal	
address	output	20	SRam Address	
data	inout	32	SRam Data	
nSRAM_BE0	output	1	SRam bankEnable 0	
nSRAM_BE1	output	1	SRam bankEnable 1	
nSRAM_BE2	output	1	SRam bankEnable 2	
nSRAM_BE3	output	1	SRam bankEnable 3	
nSRAM_WE	output	1	SRam WriteEnable	
nSRAM_CE	output	1	SRam ChipEnable	
nSRAM_OE	output	1	SRam OutputEnable	
apbi_ext	output	apb_slv_in_type	APB Slave bus input signal	
apbo_ext	input	NB_APB_SLAVE of apb_slv_out_type	APB Slave bus output signal	
ahbi_s_ext	output	ahb_slv_in_type	AHB Slave bus input signal	
ahbo_s_ext	input	NB_AHB_SLAVE of ahb_slv_out_type	AHB Slave bus output signal	
ahbi_m_ext	output	ahb_mst_In_Type	AHB Master bus input signal	
ahbo_m_ext	input	NB_AHB_MASTER of ahb_mst_out_type	AHB Master bus output signal	

## h2. AMBA Peripherals

### APB LFR Time Managment APB LFR Time Managment

LFR Time management is a real time clock. The time is give by the coarse\_time and fine\_time value. The Time management is like a big counter of 48b (coarse\_time + fine\_time). This big counter count each nb\_wait\_period of period clk49\_152MHz. The bit 0 of coarse\_time is the second.

The Time mangment can be updated by register with the value into COARSE\_TIME\_LOAD. When a space\_wire\_tick or a CTRL.force\_tick is asserted, the value into COARSE\_TIME\_LOAD is loaded in COARSE\_TIME and the FINE\_TIME is reset to 0.

APB ADDRESS	Register Name	Access	Description	Field	Reset Value
0x00	CTRL	RW	Control register	force_tick	0x0
0x04	COARSE_TIME_LOAD	RW	CoarseTime to load after the next "tick"		0x80000000
0x08	COARSE_TIME	R	Current CoarseTime		
0x0C	FINE_TIME	R	Current FineTime		

COMPONENT apb\_lfr\_time\_management\_LPP\_JCP IS  
 GENERIC(

```

pindex : INTEGER := 0;
paddr : INTEGER := 0;
pmask : INTEGER := 16###;
pirq : INTEGER := 0;
nb_wait_period : INTEGER := 375
);
PORT (
clk25MHz : IN STD_LOGIC;
clk49_152MHz : IN STD_LOGIC;
resetn : IN STD_LOGIC;
grspw_tick : IN STD_LOGIC;
apbi : IN apb_slv_in_type;
apbo : OUT apb_slv_out_type;
coarse_time : OUT STD_LOGIC_VECTOR(31 DOWNT0 0);
fine_time : OUT STD_LOGIC_VECTOR(15 DOWNT0 0)
);
END COMPONENT;
```

**Files**

File Name	Size	Date	Author
SYNC_FF.png	11.8 KB	27/02/2014	Jean-Christophe Pellion
SYNC_VALID_BIT.png	16.9 KB	27/02/2014	Jean-Christophe Pellion
edge_detection.png	10.3 KB	27/02/2014	Jean-Christophe Pellion
edge_to_level.png	12.1 KB	27/02/2014	Jean-Christophe Pellion
SYNC_VALID_BIT.png	16.9 KB	27/02/2014	Jean-Christophe Pellion
leon3_SoC.png	36.8 KB	19/03/2014	Jean-Christophe Pellion