VHDLib - Contribution_Guide - # 3

h1. Contribution Guide

You are very welcome to contribute to the VHDLib project. For any contribution you should respect the following rules.

h2. Signal naming convention

Please use meaningful names for all your signals and modules names.
Active low signals should be named with a trailing 'n', for example an active low reset should be named 'resetn'.

h2. Library structure

Any new module should be placed first in the staging folder and integrated only when it's interfaces are locked.