EQM2

Status

Differences with FM

- Different layout
- Passives parts are all industrial
- TCS not populated
- FPGA inside socket
- LVDS = **DS90LV031**/**DS90LV032** instead of **UT54LVDS031LV**/ **UT54LVDS032LV**
- No multiplexors on BIAS/ANT inputs.
- Oscillators are industrial parts not Vectron ones
- Only 8 ADCs are populated instead of 9 (HK ADC not populated)
- SCM calibration circuit not populated

LFR Wiki

Child pages:

Introduction

Context

The Laboratory of Plasma Physics(LPP) is in charge of providing the **L**ow **F**requency **R**eceiver(**LFR**) as a part of the **R**adio & **P**lasma **W**aves(RPW) instrument which will be embedded in Solar Orbiter probe. Solar Orbiter launch window is set to October 2018.

Equipment Overview

The LFR instrument is designed to produce and transmit waveforms (WF), averaged spectral matrices (ASM) and basic parameters (BP) from LF electromagnetic data (quasi DC-10kHz). The electric field data are provided by the electric antennas (ANT) and by the entity that controls their operation (BIAS). The magnetic field data are coming from the searchcoil magnetometer (SCM).
The LFR board will also have a special area reserved to the SCM Heater circuitry. LFR will monitor its own temperature and the temperature of the SCM. It will generate a calibration signal for the SCM.

Scientific Objectives and Performances

The science objective of LFR is the study of the electromagnetic wave activity in the extended corona and the solar wind, from a fraction of a Hertz to about 10 kHz, which should cover the electron gyrofrequency and most of the Doppler-shifted frequencies of the low frequency plasma waves. The main waves to be observed in this frequency range are thus kinetic or inertial Alfven waves, ion cyclotron waves, ion acoustic waves, and magnetosonic or whistler mode waves. Their characterization and the determination of their respective role in heating and accelerating the solar wind during its expansion is the main scientific issue addressed by LFR. Another important subject for LFR is the study of the low frequency plasma waves associated to solar wind disturbances, as for instance interplanetary shocks.
Characterizing the low frequency waves in the solar wind involves the capability of the LFR to distinguish solitary waves from broadband wave activity, to cover turbulence and plasma instabilities, to identify the wave modes at work. Performing a multi-component analysis of the data is thus mandatory, using either a classical Fourier analysis or another treatment of the waveforms more appropriate to turbulence analysis.
Given the limitations in the telemetry, it is necessary to implement specific techniques to take the maximum advantage of the data. The LFR is tailored to optimize the scientific return of the data. The LFR design gives the possibility of mixing different types of output data, from low-level processed data (waveform data) to high-level processed data (averaged spectral matrices and their derived parameters), with various data rate possibilities (continuous or cyclic transmission, adaptable frequency bandwidth as well as adaptable frequency and time resolutions). The scientific added value stems from the choice of the most relevant combination of the different data to be transmitted, according to the RPW Science Requirements Document (RD3). A number of predefined working modes will be defined, but it will also be possible to define other working modes in flight.

Instrument Description

Functional Description

The main functions of LFR are the following:

- Selection of 8 analog channels among 11 available.
- Sampling of 8 analog channels continuously at f0 = 24576 Hz (this includes analog anti-aliasing filtering, sampling at fs = 98304 Hz, digital anti-aliasing filtering and down-sampling at f0).
- Processing of the 8 data streams and transmission of the products to the DPU through a SpaceWire link.
- Monitoring of one SCM temperature and two LFR temperatures.
- Generation of a calibration signal for the SCM.
- Providing a reserved area on the LFR board for the SCM heater command system (design done by LPC2E, Orléans).

Hardware Description

LFR will be implemented on one PCB card inside the MEB. The block diagram is shown on Figure 1 . The LFR hardware can be divided into 3 main blocks: the analog part, the digital part and the SCM Heater part. This third part implements the means to command the SCM heating system. The design of this part is not under the responsibility of the LFR team which will only provide room for the SCM heating command board.
LFR has 11 analogue channels:

- 5 from BIAS (BIAS_1, BIAS_2, BIAS_3, BIAS_4 and BIAS_5)
- 3 from HF preamplifiers (VHF_1, VHF_2, VHF_3)
- 3 from SCM (SCM_1, SCM_2, SCM3)

LFR will digitize 8 signals among these 11 signals. The routing strategy is based on two main configurations named BIAS_WORKS and BIAS_FAILS. Whatever the configuration, the three channels coming from SCM are digitized.

The LFR analog part implements:

- The means to filter and route the 11 analog inputs. Several switches steered by the digital part allow the commutation between the BIAS_WORKS and BIAS_FAILS configurations. 8 ADCs sample continuously the selected analog channels and the data are sent to the digital part.
- The means to select and condition housekeeping data (1 temperature probe on the SCM and 2 temperature probes and the LFR).
- The means to generate a calibration signal for the SCM.
- The power supply regulation.
- The 3V voltage reference.

The digital part implements:

- An Actel RTAX4000D FPGA, more details here.
- LVDS interfaces for the SpaceWire link to the DPU.
- Memories for the FPGA.

LFR_BLOCK.png
Figure 1 LFR Block Diagram

All clock signals are derived by the FPGA logic using frequency division from two master clock frequencies generated by crystal oscillators at 50 MHz and 49.152 MHz (Figure 2). The following clock frequencies will be used on LFR:

- 25 MHz => Leon3, RAMs, AMBA bus, all other VHDL modules described in the next section
- 10 MHz => SpaceWire
- 98304 Hz => Sampling clock of the ADCs (8 main channels)

Links

RPW

LESIA's RPW website
CNES's RPW page

Solar Orbiter

CNES
ESA

RPW Contributors

RPW, LESIA
Search Coil Magnetometer(**SCM**), LPCEE
Time Domain Sampler(**TDS**), IAP
BIAS, IRF
Digital Processing Unit(**RPW-DPU**), IWF
Thermal Noise Receiver & High Frequency Receiver(**TNR-HFR**), LESIA
RPW-DPU onboard Software, LESIA

Files

SoloEM2.JPG	2.2 MB	23/05/2014	Alexis Jeandet

SoloEM2Bottom.JPG	2.22 MB	23/05/2014	Alexis Jeandet
LFR_BLOCK.png	73.5 KB	30/03/2016	Alexis Jeandet
LFR_BLOCK.png	502 KB	29/05/2018	Alexis Jeandet

A3PEModulePinout

Constraint File...Constraint File...

```
# RAM ADDRESS
set_io    {address[0]}    -pinname    H16    -fixed    yes    -DIRECTION    Inout
set_io    {address[1]}    -pinname    J15    -fixed    yes    -DIRECTION    Inout
set_io    {address[2]}    -pinname    B18    -fixed    yes    -DIRECTION    Inout
set_io    {address[3]}    -pinname    C17    -fixed    yes    -DIRECTION    Inout
set_io    {address[4]}    -pinname    C18    -fixed    yes    -DIRECTION    Inout
set_io    {address[5]}    -pinname    U2    -fixed    yes    -DIRECTION    Inout
set_io    {address[6]}    -pinname    U3    -fixed    yes    -DIRECTION    Inout
set_io    {address[7]}    -pinname    R5    -fixed    yes    -DIRECTION    Inout
set_io    {address[8]}    -pinname    N11    -fixed    yes    -DIRECTION    Inout
set_io    {address[9]}    -pinname    R13    -fixed    yes    -DIRECTION    Inout
set_io    {address[10]}    -pinname    V13    -fixed    yes    -DIRECTION    Inout
set_io    {address[11]}    -pinname    U13    -fixed    yes    -DIRECTION    Inout
set_io    {address[12]}    -pinname    V15    -fixed    yes    -DIRECTION    Inout
set_io    {address[13]}    -pinname    V16    -fixed    yes    -DIRECTION    Inout
set_io    {address[14]}    -pinname    V17    -fixed    yes    -DIRECTION    Inout
set_io    {address[15]}    -pinname    N1    -fixed    yes    -DIRECTION    Inout
set_io    {address[16]}    -pinname    R3    -fixed    yes    -DIRECTION    Inout
set_io    {address[17]}    -pinname    P4    -fixed    yes    -DIRECTION    Inout
set_io    {address[18]}    -pinname    N3    -fixed    yes    -DIRECTION    Inout
set_io    {address[19]}    -pinname    M7    -fixed    yes    -DIRECTION    Inout
# RAM DATA
set_io    {data[0]}    -pinname    P17    -fixed    yes    -DIRECTION    Inout
set_io    {data[1]}    -pinname    R18    -fixed    yes    -DIRECTION    Inout
set_io    {data[2]}    -pinname    T18    -fixed    yes    -DIRECTION    Inout
set_io    {data[3]}    -pinname    J13    -fixed    yes    -DIRECTION    Inout
set_io    {data[4]}    -pinname    T13    -fixed    yes    -DIRECTION    Inout
set_io    {data[5]}    -pinname    T12    -fixed    yes    -DIRECTION    Inout
set_io    {data[6]}    -pinname    R12    -fixed    yes    -DIRECTION    Inout
set_io    {data[7]}    -pinname    T11    -fixed    yes    -DIRECTION    Inout
set_io    {data[8]}    -pinname    N2    -fixed    yes    -DIRECTION    Inout
set_io    {data[9]}    -pinname    P1    -fixed    yes    -DIRECTION    Inout
set_io    {data[10]}    -pinname    R1    -fixed    yes    -DIRECTION    Inout
set_io    {data[11]}    -pinname    T1    -fixed    yes    -DIRECTION    Inout
set_io    {data[12]}    -pinname    M4    -fixed    yes    -DIRECTION    Inout
set_io    {data[13]}    -pinname    K1    -fixed    yes    -DIRECTION    Inout
set_io    {data[14]}    -pinname    J1    -fixed    yes    -DIRECTION    Inout
set_io    {data[15]}    -pinname    H1    -fixed    yes    -DIRECTION    Inout
set_io    {data[16]}    -pinname    H15    -fixed    yes    -DIRECTION    Inout
set_io    {data[17]}    -pinname    G15    -fixed    yes    -DIRECTION    Inout
set_io    {data[18]}    -pinname    H13    -fixed    yes    -DIRECTION    Inout
set_io    {data[19]}    -pinname    G12    -fixed    yes    -DIRECTION    Inout
set_io    {data[20]}    -pinname    V14    -fixed    yes    -DIRECTION    Inout
set_io    {data[21]}    -pinname    N9    -fixed    yes    -DIRECTION    Inout
set_io    {data[22]}    -pinname    M13    -fixed    yes    -DIRECTION    Inout
set_io    {data[23]}    -pinname    M15    -fixed    yes    -DIRECTION    Inout
set_io    {data[24]}    -pinname    J17    -fixed    yes    -DIRECTION    Inout
set_io    {data[25]}    -pinname    K15    -fixed    yes    -DIRECTION    Inout
set_io    {data[26]}    -pinname    J14    -fixed    yes    -DIRECTION    Inout
set_io    {data[27]}    -pinname    U18    -fixed    yes    -DIRECTION    Inout
set_io    {data[28]}    -pinname    H18    -fixed    yes    -DIRECTION    Inout
set_io    {data[29]}    -pinname    J18    -fixed    yes    -DIRECTION    Inout
set_io    {data[30]}    -pinname    G17    -fixed    yes    -DIRECTION    Inout
set_io    {data[31]}    -pinname    F18    -fixed    yes    -DIRECTION    Inout
# SSRAM
set_io    SRAM_BE0_bar    -pinname    U12    -fixed    yes    -DIRECTION    Inout
set_io    SRAM_BE1_bar    -pinname    K18    -fixed    yes    -DIRECTION    Inout
set_io    SRAM_BE2_bar    -pinname    K12    -fixed    yes    -DIRECTION    Inout
set_io    SRAM_BE3_bar    -pinname    F17    -fixed    yes    -DIRECTION    Inout
set_io    SRAM_WE_bar    -pinname    D18    -fixed    yes    -DIRECTION    Inout
set_io    SRAM_OE_bar    -pinname    N12    -fixed    yes    -DIRECTION    Inout
set_io    SRAM_CE    -pinname    M6    -fixed    yes    -DIRECTION    Inout
# SPW
set_io    SPW_NOM_DOUT    -pinname    C16    -fixed    yes    -DIRECTION    Inout
set_io    SPW_RED_SIN    -pinname    C15    -fixed    yes    -DIRECTION    Inout
set_io    SPW_RED_DOUT    -pinname    B7    -fixed    yes    -DIRECTION    Inout
set_io    SPW_NOM_DIN    -pinname    D6    -fixed    yes    -DIRECTION    Inout
set_io    SPW_NOM_SIN    -pinname    C6    -fixed    yes    -DIRECTION    Inout
set_io    SPW_RED_SOUT    -pinname    D7    -fixed    yes    -DIRECTION    Inout
set_io    SPW_NOM_SOUT    -pinname    C4    -fixed    yes    -DIRECTION    Inout
```

```
set_io    SPW_RED_DIN    -pinname    E6    -fixed    yes    -DIRECTION    Inout
#ADC Others
set_io    TAG1    -pinname    J12    -fixed    yes    -DIRECTION    Inout
set_io    TAG2    -pinname    K13    -fixed    yes    -DIRECTION    Inout
set_io    TAG3    -pinname    L16    -fixed    yes    -DIRECTION    Inout
set_io    TAG4    -pinname    L15    -fixed    yes    -DIRECTION    Inout
set_io    TAG5    -pinname    M16    -fixed    yes    -DIRECTION    Inout
set_io    TAG6    -pinname    L13    -fixed    yes    -DIRECTION    Inout
set_io    TAG7    -pinname    P6    -fixed    yes    -DIRECTION    Inout
set_io    TAG8    -pinname    R6    -fixed    yes    -DIRECTION    Inout
set_io    TAG9    -pinname    T4    -fixed    yes    -DIRECTION    Inout

set_io    BIAS_FAIL_SW    -pinname    A3    -fixed    yes    -DIRECTION    Inout
set_io    HK_SEL1    -pinname    A2    -fixed    yes    -DIRECTION    Inout
set_io    HK_SEL0    -pinname    C3    -fixed    yes    -DIRECTION    Inout
set_io    OEB_bar_HK    -pinname    D14    -fixed    yes    -DIRECTION    Inout
set_io    HK_SMP_CLK    -pinname    R11    -fixed    yes    -DIRECTION    Inout

set_io    OEB_bar_CH1    -pinname    A13    -fixed    yes    -DIRECTION    Inout
set_io    OEB_bar_CH2    -pinname    A14    -fixed    yes    -DIRECTION    Inout
set_io    OEB_bar_CH3    -pinname    A10    -fixed    yes    -DIRECTION    Inout
set_io    OEB_bar_CH4    -pinname    B10    -fixed    yes    -DIRECTION    Inout
set_io    OEB_bar_CH5    -pinname    B13    -fixed    yes    -DIRECTION    Inout
set_io    OEB_bar_CH6    -pinname    D13    -fixed    yes    -DIRECTION    Inout
set_io    OEB_bar_CH7    -pinname    A11    -fixed    yes    -DIRECTION    Inout
set_io    OEB_bar_CH8    -pinname    B12    -fixed    yes    -DIRECTION    Inout
set_io    SMP_CLK    -pinname    A15    -fixed    yes    -DIRECTION    Inout

set_io    SCM_CAL_EN    -pinname    A6    -fixed    yes    -DIRECTION    Inout
set_io    SYNC_bar    -pinname    B6    -fixed    yes    -DIRECTION    Inout
set_io    SCLK    -pinname    A5    -fixed    yes    -DIRECTION    Inout
set_io    DIN    -pinname    A4    -fixed    yes    -DIRECTION    Inout

set_io    ADC_D0    -pinname    A16    -fixed    yes    -DIRECTION    Inout
set_io    ADC_D1    -pinname    B16    -fixed    yes    -DIRECTION    Inout
set_io    ADC_D2    -pinname    A17    -fixed    yes    -DIRECTION    Inout
set_io    ADC_D3    -pinname    C12    -fixed    yes    -DIRECTION    Inout
set_io    ADC_D4    -pinname    B17    -fixed    yes    -DIRECTION    Inout
set_io    ADC_D5    -pinname    C13    -fixed    yes    -DIRECTION    Inout
set_io    ADC_D6    -pinname    D15    -fixed    yes    -DIRECTION    Inout
set_io    ADC_D7    -pinname    E15    -fixed    yes    -DIRECTION    Inout
set_io    ADC_D8    -pinname    D16    -fixed    yes    -DIRECTION    Inout
set_io    ADC_D9    -pinname    F16    -fixed    yes    -DIRECTION    Inout
set_io    ADC_D10    -pinname    F15    -fixed    yes    -DIRECTION    Inout
set_io    ADC_D11    -pinname    G16    -fixed    yes    -DIRECTION    Inout
set_io    ADC_D12    -pinname    F13    -fixed    yes    -DIRECTION    Inout
set_io    ADC_D13    -pinname    G13    -fixed    yes    -DIRECTION    Inout

set_io    LED0    -pinname    K17    -fixed    yes    -DIRECTION    Inout
set_io    LED1    -pinname    L18    -fixed    yes    -DIRECTION    Inout
set_io    LED2    -pinname    M17    -fixed    yes    -DIRECTION    Inout

set_io    clk_49_152MHz    -pinname    D5    -fixed    yes    -DIRECTION    Inout
set_io    clk_50_000MHz    -pinname    B3    -fixed    yes    -DIRECTION    Inout

set_io    Reset    -pinname    N18    -fixed    yes    -DIRECTION    Inout
set_io    BP0    -pinname    N17    -fixed    yes    -DIRECTION    Inout
set_io    BP1    -pinname    P18    -fixed    yes    -DIRECTION    Inout
```

Calibrations

PFM Calibrations

Transfer Function

1) Transfer Functions @F0

For the whole test we will use the following parameters:

- LFR mode= Normal Mode
- ASM period = 4s
- Snapshots period = 22s
- Input signal amplitude 3Vp

a) Low Frequencies and FFT frequencies

7 frequencies: from 12Hz to 84Hz with Δf = 12Hz
128 frequencies: from 96Hz to 12288Hz with Δf = 96Hz

View measurements...View measurements...

Channels	Parameters	Curves	data
B1 and B2	BIAS Work = 1 R0=R1=R2 = 1 SP0=SP1 = 0	TF1aB1B2_2016-03-29T10_10_31.781731.svg	Result files
B2 and B3	BIAS Work = 1 R0=R1=R2 = 1 SP0=SP1 = 0	TF1aB2B3_2016-03-29T11_22_47.937601.svg	Result files
B3 and BIAS1	BIAS Work = 1 R0=R1=R2 = 1 SP0=SP1 = 0	TF1aB3BIAS1_2016-03-29T14_42_16.973207.svg	Result files
BIAS1 and BIAS2	BIAS Work = 1 R0=R1=R2 = 1 SP0=SP1 = 0	TF1aBIAS1BIAS2_2016-03-29T15_37_41.119563.svg	Result files
BIAS2 and BIAS3	BIAS Work = 1 R0=R1=R2 = 1 SP0=SP1 = 0	TF1aBIAS2BIAS3_2016-03-29T16_33_14.886467.svg	Result files
BIAS1 and BIAS4	BIAS Work = 1 R0=R1=R2 = 0 SP0=SP1 = 0	TF1aBIAS1BIAS4_2016-03-29T13_48_36.670741.svg	Result files
BIAS4 and BIAS5	BIAS Work = 1 R0=R1=R2 = 0 SP0=SP1 = 0	TF1aBIAS4BIAS5_2016-03-29T17_36_37.811434.svg	Result files
B1, B2, B3, BIAS1, BIAS2 (φ = 90°), BIAS3 (φ = 90°)	BIAS Work = 1 R0=R1=R2 = 1 SP0=SP1 = 1	TF1aB1B2B3BIA1BIA290BIA390_2016-03-29T18_40_30.458240.svg	Result files
B1, B2, B3, VHF1, VHF2, VHF3	BIAS Work = 0 R0=R1=R2 = 1 SP0=SP1 = 0	TF1aB1B2B3V1V2V3_2016-03-29T19_34_42.946732.svg	Result files

b) Frequencies > F0/2

24 frequencies: from 13056Hz to 30720Hz with Δf = 768Hz

View measurements...View measurements...

Channels	Parameters	Curves	data
B1, B2, B3, BIAS1, BIAS2 and BIAS3	BIAS Work = 1 R0=R1=R2 = 1 SP0=SP1 = 0		Result files
B1, B2, B3, BIAS1, BIAS4, BIAS5	BIAS Work = 1 R0=R1=R2 = 0 SP0=SP1 = 0		Result files
B1, B2, B3, BIAS1, BIAS2 (φ = 90°) and BIAS3 (φ	BIAS Work = 1 R0=R1=R2 = 1		Result files

= 90°)	SP0=SP1 = 1		
B1, B2, B3, VHF1, VHF2 and VHF3	BIAS Work = 0 R0=R1=R2 = 1 SP0=SP1 = 0		Result files
B1, B2, B3, VHF1, VHF2 (φ = 90°) and VHF3 (φ = 90°)	BIAS Work = 0 R0=R1=R2 = 1 SP0=SP1 = 1		Result files

2) Transfer Functions @F1

a) Low Frequencies

- LFR mode= SBM1
- ASM period = 32s
- Snapshots period = 32s
- Input signal amplitude 3Vp
- Step duration = 420s

10 frequencies: from 0.01Hz to 0.1Hz with Δf = 0.01Hz

View measurements...View measurements...

Channels	Parameters	Curves	data
B1, B2, B3, BIAS1, BIAS2 and BIAS3	BIAS Work = 1 R0=R1=R2 = 1 SP0=SP1 = 0		Result files
B1, B2, B3, BIAS1, BIAS4 and BIAS5	BIAS Work = 1 R0=R1=R2 = 0 SP0=SP1 = 0		Result files
B1, B2, B3, BIAS1, BIAS2 (φ = 90°) and BIAS3 (φ = 90°)	BIAS Work = 1 R0=R1=R2 = 1 SP0=SP1 = 1		Result files

---

- LFR mode= SBM1
- ASM period = 4s
- Snapshots period = 32s
- Input signal amplitude 3Vp
- Step duration = 32s

10 frequencies: from 0.2Hz to 2Hz with Δf = 0.2Hz
6 frequencies: from 4Hz to 14Hz with Δf = 2Hz

View measurements...View measurements...

Channels	Parameters	Curves	data
B1, B2, B3, BIAS1, BIAS2, BIAS3	BIAS Work = 1 R0=R1=R2 = 1 SP0=SP1 = 0		Result files
B1, B2, B3, BIAS1, BIAS4, BIAS5	BIAS Work = 1 R0=R1=R2 = 0 SP0=SP1 = 0		Result files
B1, B2, B3, BIAS1, BIAS2 (φ = 90°) and BIAS3 (φ = 90°)	BIAS Work = 1 R0=R1=R2 = 1 SP0=SP1 = 1		Result files

b) FFT frequencies

- LFR mode= SBM1
- ASM period = 4s
- Snapshots period = 32s
- Input signal amplitude 3Vp
- Step duration = 32s

128 frequencies: from 16Hz to 2048Hz with Δf = 16Hz

View measurements...View measurements...

Channels	Parameters	Curves	data
B1, B2, B3, BIAS1, BIAS2 and BIAS3	BIAS Work = 1 R0=R1=R2 = 1 SP0=SP1 = 0	TF2bB1B2B3BIAS1BIAS2BIAS3_2016-03-30T18_17_58.746031.svg	Result files
B1, B2, B3, BIAS1, BIAS4 and BIAS5	BIAS Work = 1 R0=R1=R2 = 0 SP0=SP1 = 0	TF2bB1B2B3BIAS1BIAS4BIAS5_2016-03-30T19_41_32.077592.svg	Result files
B1, B2, B3, BIAS1, BIAS2 (φ = 90°) and BIAS3 (φ = 90°)	BIAS Work = 1 R0=R1=R2 = 1 SP0=SP1 = 1	TF2bB1B2B3BIAS1BIAS290BIAS390_2016-03-31T09_43_31.908069.svg	Result files
B1, B2, B3, VHF1, VHF2 and VHF3	BIAS Work = 0 R0=R1=R2 = 1 SP0=SP1 = 0	TF2bB1B2B3V1V2V3_2016-03-31T10_56_48.227834.svg	Result files
B1, B2, B3, VHF1, VHF2 (φ = 90°) and VHF3 (φ = 90°)	BIAS Work = 0 R0=R1=R2 = 1 SP0=SP1 = 1	TF2bB1B2B3V1V290V390_2016-03-31T12_22_38.041766.svg	Result files

3) Transfer Functions @F2 and @F3 (0.01Hz-0.1Hz + 0.125Hz-0.875Hz)

a) Low Frequencies

- LFR mode= SBM2
- ASM period = 32s
- Snapshots period = 32s
- Input signal amplitude 3Vp
- Step duration = 420s

10 frequencies: from 0.01Hz to 0.1Hz with Δf = 0.01Hz

View measurements...View measurements...

Channels	Parameters	Curves	data
B1, B2, B3, BIAS1, BIAS2 and BIAS3	BIAS Work = 1 R0=R1=R2 = 1 SP0=SP1 = 0		Result files
B1, B2, B3, BIAS1, BIAS4 and BIAS5	BIAS Work = 1 R0=R1=R2 = 0 SP0=SP1 = 0		Result files
B1, B2, B3, BIAS1, BIAS2 (φ = 90°) and BIAS3 (φ = 90°)	BIAS Work = 1 R0=R1=R2 = 1 SP0=SP1 = 1		"Result files": **SKIPPED**

- LFR mode= SBM2
- ASM period = 32s
- Snapshots period = 32s
- Input signal amplitude 3Vp
- Step duration = 360s

7 frequencies: from 0.125Hz to 0.875Hz with Δf = 0.125Hz

View measurements...View measurements...

Channels	Parameters	Curves	data
B1, B2, B3, BIAS1, BIAS2 and BIAS3	BIAS Work = 1 R0=R1=R2 = 1 SP0=SP1 = 0		Result files
B1, B2, B3, BIAS1, BIAS2 (φ = 90°) and BIAS3 (φ	BIAS Work = 1 R0=R1=R2 = 1		Result files

= 90°)	SP0=SP1 = 1		

- LFR mode= SBM2
- ASM period = 4s
- Snapshots period = 22s
- Input signal amplitude 3Vp
- Step duration = 44s

7 frequencies: from 0.125Hz to 0.875Hz with Δf = 0.125Hz

View measurements...View measurements...

Channels	Parameters	Curves	data
B1, B2, B3, BIAS1, BIAS4 and BIAS5	BIAS Work = 1 R0=R1=R2 = 0 SP0=SP1 = 0		Result files

b) FFT frequencies

- LFR mode= SBM2
- ASM period = 4s
- Snapshots period = 22s
- Input signal amplitude 3Vp
- Step duration = 22s

128 frequencies: from 1Hz to 128Hz with Δf = 1Hz

View measurements...View measurements...

Channels	Parameters	Curves	data
B1, B2, B3, BIAS1, BIAS2 and BIAS3	BIAS Work = 1 R0=R1=R2 = 1 SP0=SP1 = 0	TF3bB1B2B3BIAS1BIAS2BIAS3_2016-03-31T19_52_13.463634.svg	Result files
B1, B2, B3, BIAS1, BIAS4, BIAS5	BIAS Work = 1 R0=R1=R2 = 0 SP0=SP1 = 0	TF3bB1B2B3BIAS1BIAS4BIAS5_2016-03-31T20_41_42.933912.svg	Result files
B1, B2, B3, BIAS1, BIAS2 (φ = 90°) and BIAS3 (φ = 90°)	BIAS Work = 1 R0=R1=R2 = 1 SP0=SP1 = 1	TF3bB1B2B3BIAS1BIAS290BIAS390_2016-03-31T21_30_30.341444.svg	Result files
B1, B2, B3, VHF1, VHF2 and VHF3	BIAS Work = 0 R0=R1=R2 = 1 SP0=SP1 = 0	TF3bB1B2B3V1V2V3_2016-04-01T09_28_48.231276.svg	Result files
B1, B2, B3, VHF1, VHF2 (φ = 90°) and VHF3 (φ = 90°)	BIAS Work = 0 R0=R1=R2 = 1 SP0=SP1 = 1	TF3bB1B2B3V1V290V390_2016-04-01T10_18_06.144607.svg	Result files

4) Transfer Functions @F3

a) F3 specific frequencies (+ partial redundancy with F2)

- LFR mode= SBM2
- ASM period = 32s
- Snapshots period = 32s
- Input signal amplitude 3Vp
- Step duration = 360s

15 frequencies: from 1Hz to 8Hz with Δf = 0.5Hz

View measurements...View measurements...

Channels	Parameters	Curves	data
B1, B2, B3, BIAS1,	BIAS Work = 1		Result files

BIAS2 and BIAS3	R0=R1=R2 = 1 SP0=SP1 = 0		
B1, B2, B3, BIAS1, BIAS2 (φ = 90°) and BIAS3 (φ = 90°)	BIAS Work = 1 R0=R1=R2 = 1 SP0=SP1 = 1		Result files

b) Frequencies > F3/2

- LFR mode= SBM2
- ASM period = 32s
- Snapshots period = 32s
- Input signal amplitude 3Vp
- Step duration = 180s

12 frequencies: from 9Hz to 20Hz with Δf = 1Hz

View measurements...View measurements...

Channels	Parameters	Curves	data
B1, B2, B3, BIAS1, BIAS2 and BIAS3	BIAS Work = 1 R0=R1=R2 = 1 SP0=SP1 = 0		Result files
B1, B2, B3, BIAS1, BIAS2 (φ = 90°) and BIAS3 (φ = 90°)	BIAS Work = 1 R0=R1=R2 = 1 SP0=SP1 = 1		Result files

Files

TF1_a_B1B2.tar.bz2	4.02 MB	29/03/2016	Alexis Jeandet
TF1_a_B1B2B3BIA1BIA290BIA390.tar.bz2	6.37 MB	29/03/2016	Alexis Jeandet
TF1_a_B2B3.tar.bz2	4.25 MB	29/03/2016	Alexis Jeandet
TF1_a_B3BIAS1.tar.bz2	4.29 MB	29/03/2016	Alexis Jeandet
TF1_a_BIAS1BIAS2.tar.bz2	4.19 MB	29/03/2016	Alexis Jeandet
TF1_a_BIAS1BIAS4.tar.bz2	4.16 MB	29/03/2016	Alexis Jeandet
TF1_a_BIAS2BIAS3.tar.bz2	4 MB	29/03/2016	Alexis Jeandet
TF1_a_BIAS4BIAS5.tar.bz2	4.14 MB	29/03/2016	Alexis Jeandet
TF1_a_B1B2B3V1V2V3.tar.bz2	5.74 MB	29/03/2016	Alexis Jeandet
TF1_b_B1B2B3BIAS1BIAS2BIAS3.tar.bz2	1.21 MB	30/03/2016	Alexis Jeandet
TF1_b_B1B2B3BIAS1BIAS4BIAS5.tar.bz2	1.19 MB	30/03/2016	Alexis Jeandet
TF1_b_B1B2B3V1V290V390.tar.bz2	1.33 MB	30/03/2016	Alexis Jeandet
TF1_b_B1B2B3BIAS1BIAS290BIAS390.tar.bz2	1.35 MB	30/03/2016	Alexis Jeandet
TF1_b_B1B2B3V1V2V3.tar.bz2	1.17 MB	30/03/2016	Alexis Jeandet
TF2_a_B1B2B3BIAS1BIAS2BIAS3.tar.bz2	138 MB	30/03/2016	Alexis Jeandet
TF2_a_B1B2B3BIAS1BIAS4BIAS5.tar.bz2	134 MB	30/03/2016	Alexis Jeandet
TF2_a_B1B2B3BIAS1BIAS290BIAS390.tar.bz2	150 MB	30/03/2016	Alexis Jeandet
TF2_a_bis_B1B2B3BIAS1BIAS2BIAS3.tar.bz2	23.1 MB	30/03/2016	Alexis Jeandet
TF2_a_bis_B1B2B3BIAS1BIAS4BIAS5.tar.bz2	24.6 MB	30/03/2016	Alexis Jeandet
TF2_a_bis_B1B2B3BIAS1BIAS290BIAS390.tar.bz2	25.7 MB	30/03/2016	Alexis Jeandet
TF2_b_B1B2B3BIAS1BIAS2BIAS3.tar.7z	134 MB	30/03/2016	Alexis Jeandet
TF2_b_B1B2B3BIAS1BIAS4BIAS5.tar.7z	140 MB	30/03/2016	Alexis Jeandet
TF1aB2B3_2016-03-29T11_22_47.937601.svg	138 KB	31/03/2016	Alexis Jeandet
TF1aB3BIAS1_2016-03-29T14_42_16.973207.svg	132 KB	31/03/2016	Alexis Jeandet
TF1aB1B2_2016-03-29T10_10_31.781731.svg	137 KB	31/03/2016	Alexis Jeandet
TF1aBIAS1BIAS2_2016-03-29T15_37_41.119563.svg	138 KB	31/03/2016	Alexis Jeandet
TF1aBIAS1BIAS4_2016-03-29T13_48_36.670741.svg	138 KB	31/03/2016	Alexis Jeandet
TF1aBIAS2BIAS3_2016-03-29T16_33_14.886467.svg	138 KB	31/03/2016	Alexis Jeandet
TF1aBIAS4BIAS5_2016-03-29T17_36_37.811434.svg	137 KB	31/03/2016	Alexis Jeandet

TF2_b_B1B2B3V1V2V3.tar.7z	133 MB	31/03/2016	Alexis Jeandet
TF2_b_B1B2B3BIAS1BIAS290BIAS390.tar.7z	142 MB	31/03/2016	Alexis Jeandet
TF3_a_B1B2B3BIAS1BIAS2BIAS3.tar.7z	11.9 MB	31/03/2016	Alexis Jeandet
TF2_b_B1B2B3V1V290V390.tar.7z	138 MB	31/03/2016	Alexis Jeandet
TF3_a_B1B2B3BIAS1BIAS4BIAS5.tar.7z	12 MB	31/03/2016	Alexis Jeandet
TF3_a_ter_B1B2B3BIAS1BIAS4BIAS5.tar.7z	1.77 MB	31/03/2016	Alexis Jeandet
TF3_a_bis_B1B2B3BIAS1BIAS2BIAS3.tar.7z	8.46 MB	31/03/2016	Alexis Jeandet
TF3_a_bis_B1B2B3BIAS1BIAS290BIAS390.tar.7z	8.89 MB	31/03/2016	Alexis Jeandet
TF3_b_B1B2B3BIAS1BIAS2BIAS3.tar.7z	18.5 MB	31/03/2016	Alexis Jeandet
TF3_b_B1B2B3BIAS1BIAS290BIAS390.tar.7z	21.1 MB	31/03/2016	Alexis Jeandet
TF3_b_B1B2B3BIAS1BIAS4BIAS5.tar.7z	19 MB	31/03/2016	Alexis Jeandet
TF3_b_B1B2B3V1V2V3.tar.7z	18.3 MB	01/04/2016	Alexis Jeandet
TF3_b_B1B2B3V1V290V390.tar.7z	18.3 MB	01/04/2016	Alexis Jeandet
TF4_b_B1B2B3BIAS1BIAS2BIAS3.tar.7z	7.66 MB	01/04/2016	Alexis Jeandet
TF4_a_B1B2B3BIAS1BIAS2BIAS3.tar.7z	18.7 MB	01/04/2016	Alexis Jeandet
TF4_a_B1B2B3BIAS1BIAS290BIAS390.tar.7z	19.7 MB	01/04/2016	Alexis Jeandet
TF1aB1B2B3V1V2V3_2016-03-29T19_34_42.946732.svg	291 KB	01/04/2016	Alexis Jeandet
TF1aB1B2B3BIA1BIA290BIA390_2016-03-29T18_40_30.458240.svg	292 KB	01/04/2016	Alexis Jeandet
TF2bB1B2B3BIAS1BIAS2BIAS3_2016-03-30T18_17_58.746031.svg	272 KB	01/04/2016	Alexis Jeandet
TF2bB1B2B3BIAS1BIAS4BIAS5_2016-03-30T19_41_32.077592.svg	273 KB	01/04/2016	Alexis Jeandet
TF2bB1B2B3V1V2V3_2016-03-31T10_56_48.227834.svg	273 KB	01/04/2016	Alexis Jeandet
TF2bB1B2B3BIAS1BIAS290BIAS390_2016-03-31T09_43_31.908069.svg	274 KB	01/04/2016	Alexis Jeandet
TF2bB1B2B3V1V290V390_2016-03-31T12_22_38.041766.svg	269 KB	01/04/2016	Alexis Jeandet
TF4_b_B1B2B3BIAS1BIAS290BIAS390.tar.7z	8.11 MB	01/04/2016	Alexis Jeandet
TF3bB1B2B3BIAS1BIAS2BIAS3_2016-03-31T19_52_13.463634.svg	276 KB	01/04/2016	Alexis Jeandet
TF3bB1B2B3BIAS1BIAS4BIAS5_2016-03-31T20_41_42.933912.svg	273 KB	01/04/2016	Alexis Jeandet
TF3bB1B2B3V1V2V3_2016-04-01T09_28_48.231276.svg	275 KB	01/04/2016	Alexis Jeandet
TF3bB1B2B3BIAS1BIAS290BIAS390_2016-03-31T21_30_30.341444.svg	273 KB	01/04/2016	Alexis Jeandet
TF3bB1B2B3V1V290V390_2016-04-01T10_18_06.144607.svg	273 KB	01/04/2016	Alexis Jeandet
TF3aterB1B2B3BIAS1BIAS4BIAS5_2016-03-31T18_12_05.951507.svg	78.7 KB	04/04/2016	thomas chust

SPARE Calibrations

Python scrip to build archives

```
import sys
import os
import shutil
import path
from glob import glob
from lfrcompliance.test_engine.testcontext import *
from lfrcompliance.test_engine.result_loader import *
OUTPUT_FOLDER="/run/media/jeandet/key64/OwnCloud/TESTS_LFR_SPARE_CALIBRATIONS/scripts/tests/inputs/"

files=glob.glob(OUTPUT_FOLDER+"/TF*.output")

os.chdir("/home/jeandet/Documents/temp")
for file in files:
    res=ResultLoader(file)
    if len(res.PacketsRecords):
        print(res.PacketsRecords)
        archive=os.path.basename(file).split('_')[0]
        print(os.path.basename(file).split('_')[0])
        os.mkdir(archive)
        shutil.copy(res.PacketsRecords[0],archive+"/")
        shutil.copy(file,archive+"/")
        print(os.system("tar cv  {} | 7z a -si -m0=LZMA2 -mx=9 -mmt=on -aoa -mfb=64 {}.tar.7z".format(archive,
archive)))
        shutil.rmtree(archive)
```

Transfer Function

1) Transfer Functions @F0

For the whole test we will use the following parameters:

- LFR mode= Normal Mode
- ASM period = 4s
- Snapshots period = 22s
- Input signal amplitude 1.4Vp

a) Low Frequencies and FFT frequencies

7 frequencies: from 12Hz to 84Hz with Δf = 12Hz
128 frequencies: from 96Hz to 12288Hz with Δf = 96Hz

View measurements...View measurements...

Channels	Parameters	Curves	data
B1 and B2	BIAS Work = 1 R0=R1=R2 = 1 SP0=SP1 = 0		Result files
B2 and B3	BIAS Work = 1 R0=R1=R2 = 1 SP0=SP1 = 0		Result files
B3 and BIAS1	BIAS Work = 1 R0=R1=R2 = 1 SP0=SP1 = 0		Result files
BIAS1 and BIAS2	BIAS Work = 1 R0=R1=R2 = 1 SP0=SP1 = 0		Result files
BIAS2 and BIAS3	BIAS Work = 1 R0=R1=R2 = 1 SP0=SP1 = 0		Result files
BIAS1 and BIAS4	BIAS Work = 1 R0=R1=R2 = 0 SP0=SP1 = 0		Result files
BIAS4 and BIAS5	BIAS Work = 1 R0=R1=R2 = 0 SP0=SP1 = 0		Result files

B1, B2, B3, BIAS1, BIAS2 (φ = 90°), BIAS3 (φ = 90°)	BIAS Work = 1 R0=R1=R2 = 1 SP0=SP1 = 1		Result files
B1, B2, B3, VHF1, VHF2, VHF3	BIAS Work = 0 R0=R1=R2 = 1 SP0=SP1 = 0		Result files

b) Frequencies > F0/2

24 frequencies: from 13056Hz to 30720Hz with Δf = 768Hz

View measurements...View measurements...

Channels	Parameters	Curves	data
B1, B2, B3, BIAS1, BIAS2 and BIAS3	BIAS Work = 1 R0=R1=R2 = 1 SP0=SP1 = 0		Result files
B1, B2, B3, BIAS1, BIAS4, BIAS5	BIAS Work = 1 R0=R1=R2 = 0 SP0=SP1 = 0		Result files
B1, B2, B3, BIAS1, BIAS2 (φ = 90°) and BIAS3 (φ = 90°)	BIAS Work = 1 R0=R1=R2 = 1 SP0=SP1 = 1		Result files
B1, B2, B3, VHF1, VHF2 and VHF3	BIAS Work = 0 R0=R1=R2 = 1 SP0=SP1 = 0		Result files
B1, B2, B3, VHF1, VHF2 (φ = 90°) and VHF3 (φ = 90°)	BIAS Work = 0 R0=R1=R2 = 1 SP0=SP1 = 1		Result files

2) Transfer Functions @F1

a) Low Frequencies

- LFR mode= SBM1
- ASM period = 32s
- Snapshots period = 32s
- Input signal amplitude 3Vp
- Step duration = 420s

10 frequencies: from 0.01Hz to 0.1Hz with Δf = 0.01Hz

View measurements...View measurements...

Channels	Parameters	Curves	data
B1, B2, B3, BIAS1, BIAS2 and BIAS3	BIAS Work = 1 R0=R1=R2 = 1 SP0=SP1 = 0		Result files
B1, B2, B3, BIAS1, BIAS4 and BIAS5	BIAS Work = 1 R0=R1=R2 = 0 SP0=SP1 = 0		"Result files":MISSING
B1, B2, B3, BIAS1, BIAS2 (φ = 90°) and BIAS3 (φ = 90°)	BIAS Work = 1 R0=R1=R2 = 1 SP0=SP1 = 1		"Result files":MISSING

Files

TF1aB1B2.tar.7z	6.88 MB	15/05/2016	Alexis Jeandet
TF1aB1B2B3BIA1BIA290BIA390.tar.7z	9.3 MB	15/05/2016	Alexis Jeandet

TF1aB2B3.tar.7z	6.95 MB	15/05/2016	Alexis Jeandet
TF1aB1B2B3V1V2V3.tar.7z	8.32 MB	15/05/2016	Alexis Jeandet
TF1aB3BIAS1.tar.7z	6.43 MB	15/05/2016	Alexis Jeandet
TF1aBIAS1BIAS2.tar.7z	6.53 MB	15/05/2016	Alexis Jeandet
TF1aBIAS1BIAS4.tar.7z	6.33 MB	15/05/2016	Alexis Jeandet
TF1aBIAS2BIAS3.tar.7z	6.51 MB	15/05/2016	Alexis Jeandet
TF1bB1B2B3BIAS1BIAS2BIAS3.tar.7z	1.07 MB	15/05/2016	Alexis Jeandet
TF1aBIAS4BIAS5.tar.7z	6.26 MB	15/05/2016	Alexis Jeandet
TF1bB1B2B3V1V290V390.tar.7z	1.18 MB	15/05/2016	Alexis Jeandet
TF1bB1B2B3BIAS1BIAS4BIAS5.tar.7z	1.02 MB	15/05/2016	Alexis Jeandet
TF1bB1B2B3BIAS1BIAS290BIAS390.tar.7z	1.22 MB	15/05/2016	Alexis Jeandet
TF1bB1B2B3V1V2V3.tar.7z	1.05 MB	15/05/2016	Alexis Jeandet
TF2aB1B2B3BIAS1BIAS2BIAS3.tar.7z	72.3 MB	15/05/2016	Alexis Jeandet
TF1aB1B2B3V1V2V3.tar.7z	8.26 MB	14/06/2016	Alexis Jeandet
TF2aB1B2B3BIAS1BIAS4BIAS5.tar.7z	143 MB	14/06/2016	Alexis Jeandet
TF2abisB1B2B3BIAS1BIAS2BIAS3.tar.7z	13.1 MB	14/06/2016	Alexis Jeandet
TF2aB1B2B3BIAS1BIAS290BIAS390.tar.7z	72 MB	14/06/2016	Alexis Jeandet
TF2bB1B2B3BIAS1BIAS2BIAS3.tar.7z	113 MB	14/06/2016	Alexis Jeandet
TF2bB1B2B3BIAS1BIAS4BIAS5.tar.7z	111 MB	14/06/2016	Alexis Jeandet
TF2bB1B2B3BIAS1BIAS290BIAS390.tar.7z	109 MB	14/06/2016	Alexis Jeandet
TF2bB1B2B3V1V2V3.tar.7z	107 MB	14/06/2016	Alexis Jeandet
TF3aB1B2B3BIAS1BIAS2BIAS3.tar.7z	12.7 MB	14/06/2016	Alexis Jeandet
TF3aB1B2B3BIAS1BIAS4BIAS5.tar.7z	12.4 MB	14/06/2016	Alexis Jeandet
TF3aB1B2B3BIAS1BIAS290BIAS390.tar.7z	11.5 MB	14/06/2016	Alexis Jeandet
TF2bB1B2B3V1V290V390.tar.7z	106 MB	14/06/2016	Alexis Jeandet
TF3abisB1B2B3BIAS1BIAS290BIAS390.tar.7z	7.97 MB	14/06/2016	Alexis Jeandet
TF3abisB1B2B3BIAS1BIAS2BIAS3.tar.7z	8.07 MB	14/06/2016	Alexis Jeandet
TF3aterB1B2B3BIAS1BIAS4BIAS5.tar.7z	1.44 MB	14/06/2016	Alexis Jeandet
TF3bB1B2B3BIAS1BIAS4BIAS5.tar.7z	16.6 MB	14/06/2016	Alexis Jeandet
TF3bB1B2B3BIAS1BIAS2BIAS3.tar.7z	18.1 MB	14/06/2016	Alexis Jeandet
TF3bB1B2B3BIAS1BIAS290BIAS390.tar.7z	16.3 MB	14/06/2016	Alexis Jeandet
TF3bB1B2B3V1V2V3.tar.7z	15.6 MB	14/06/2016	Alexis Jeandet
TF3bB1B2B3V1V290V390.tar.7z	15.9 MB	14/06/2016	Alexis Jeandet
TF4aB1B2B3BIAS1BIAS2BIAS3.tar.7z	16.6 MB	14/06/2016	Alexis Jeandet
TF4aB1B2B3BIAS1BIAS290BIAS390.tar.7z	16.3 MB	14/06/2016	Alexis Jeandet
TF4bB1B2B3BIAS1BIAS290BIAS390.tar.7z	6.8 MB	14/06/2016	Alexis Jeandet
TF4bB1B2B3BIAS1BIAS2BIAS3.tar.7z	7.83 MB	14/06/2016	Alexis Jeandet

Pictures

P1020368.JPG

P1020085.JPG

2013_06_06_11_02_19.jpg

P1010945.JPG

Files

P1020368.JPG	4.77 MB	15/09/2014	Alexis Jeandet
P1020085.JPG	3.45 MB	15/09/2014	Alexis Jeandet
P1010945.JPG	4.16 MB	15/09/2014	Alexis Jeandet
2013_06_06_11_02_19.jpg	1.46 MB	15/09/2014	Alexis Jeandet

RTAX Prototyping

To prototype the Actel's RTAX4000D on our design we use tree solutions, one home made and two made by Ironwood Electronics .
We used the first home made solution for our engineering model because this solution is cheap and allow us to use only one A3PE3000 fpga and is compatible with RTAX4000D pinout. The second solution is an improved version of the first one. This second solution is easier to remove if we want to solder a RTAX4000D-proto on the same board. The third solution allow us to test a RTAX4000D in tie-bar without soldering for tests such as **P**ost **P**rogramming **B**urn **I**n (PPBI).

First solution (home made)

You can easily get source files of this socket here: RTAX To A3PE Converter
The main drawback of this solution is that this socket isn't easy to solder.

SocketLPPTop.jpg	SocketLPPSide.jpg	SocketLPPonEM.JPG

Second solution (Ironwood)

This solution has the same pinout than previous one.

SocketManudaxTop.JPG	SocketManudaxSide.JPG	LFR_EQM.JPG

Third solution (Ironwood)

Ironwood pruduct page

This solution allow solderless testing of your FPGA in **tie-bar**. This also allows you check your flight model board with a cheaper proto FPGA before doing anything with flight FPGA. Note that this socket needs holes on your PCB and takes some space on your PCB.

EQM2_TOP.jpg	EQM2_SIDE.jpg	EQM2_SOCKET_OPENED.jpg

Files

SocketLPPonEM.JPG	3.45 MB	26/03/2015	Alexis Jeandet
SocketLPPSide.jpg	1.46 MB	26/03/2015	Alexis Jeandet
LFR_EQM.JPG	5.2 MB	26/03/2015	Alexis Jeandet
SocketLPPTop.jpg	1.5 MB	26/03/2015	Alexis Jeandet
SocketManudaxSide.JPG	4.55 MB	26/03/2015	Alexis Jeandet
SocketManudaxTop.JPG	4.66 MB	26/03/2015	Alexis Jeandet
EQM2_SIDE.jpg	613 KB	29/03/2016	Alexis Jeandet
EQM2_SOCKET_OPENED.jpg	871 KB	29/03/2016	Alexis Jeandet
EQM2_TOP.jpg	851 KB	29/03/2016	Alexis Jeandet

Schematics

Top level

QM_SOLO_LFR-01.08-TOP.jpg

Power supply

QM_SOLO_LFR-01.08-PWR.jpg

Input buffer

QM_SOLO_LFR-01.08-BUFF.jpg
QM_SOLO_LFR-01.08-AN.jpg

Bias fail multiplexers

QM_SOLO_LFR-01.08-BFAIL.jpg

ADCs

QM_SOLO_LFR-01.08-ADC.jpg

Search Coil callibration

QM_SOLO_LFR-01.08-CAL.jpg

Housekeepings

QM_SOLO_LFR-01.08-HK.jpg

FPGA

QM_SOLO_LFR-01.08-FPGA.jpg

SRAM

QM_SOLO_LFR-01.08-SRAM.jpg

Spacewire

QM_SOLO_LFR-01.08-SPW.jpg

Changelog

QM_SOLO_LFR-01.08-Changelog.jpg

Files

QM_SOLO_LFR-01.08-AN.jpg	1.35 MB	16/10/2014	Alexis Jeandet
QM_SOLO_LFR-01.08-ADC.jpg	2.55 MB	16/10/2014	Alexis Jeandet
QM_SOLO_LFR-01.08-BFAIL.jpg	1.42 MB	16/10/2014	Alexis Jeandet
QM_SOLO_LFR-01.08-CAL.jpg	2.18 MB	16/10/2014	Alexis Jeandet
QM_SOLO_LFR-01.08-BUFF.jpg	1.95 MB	16/10/2014	Alexis Jeandet
QM_SOLO_LFR-01.08-Changelog.jpg	2.13 MB	16/10/2014	Alexis Jeandet
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QM_SOLO_LFR-01.08-FPGA.jpg	2.86 MB	16/10/2014	Alexis Jeandet
QM_SOLO_LFR-01.08-SPW.jpg	1.44 MB	16/10/2014	Alexis Jeandet
QM_SOLO_LFR-01.08-PWR.jpg	2.32 MB	16/10/2014	Alexis Jeandet
QM_SOLO_LFR-01.08-TOP.jpg	2.89 MB	16/10/2014	Alexis Jeandet
QM_SOLO_LFR-01.08-SRAM.jpg	2.11 MB	16/10/2014	Alexis Jeandet