VHDLib - Bug #96

DMA latency to access External memory

18/03/2014 10:18 AM - Jean-Christophe Pellion

Status:	Rejected	**Start date:**	18/03/2014
Priority:	Normal	**Due date:**	
Assignee:	Jean-Christophe Pellion	**% Done:**	0%
Category:		**Estimated time:**	0.00 hour
Target version:		**Spent time:**	0.00 hour
revision:	r0		

Description

1- Verify than there is too waitstate access during a Memory Burst Access
2- Try others configurations to limit this latency ...

History

#1 - 02/12/2016 01:10 PM - Jean-Christophe Pellion

- Status changed from New to Rejected