

LFR-FSW - Bug #77

Reset HW met à 0 le bit MSB du temps interne (qui représente la synchronisation avec un "time code")

06/03/2014 04:11 PM - Gerald Saule

Status:	Closed	Start date:	06/03/2014
Priority:	Normal	Due date:	
Assignee:	bruno katra	% Done:	0%
Category:		Estimated time:	0.00 hour
Target version:		Spent time:	0.00 hour
revision:	r104		

Description

Un reset HW met le champ TIME à 0, donc en particulier le bit MSB qui représente la synchronisation avec un "time code". Cela provoque alors l'émission immédiate des HKs sans prise en compte des "time code" et SY_LFR_TIME_SYN_TIMEOUT.

Contexte:
LPPMON Version=0.2.2 - Branch=default - Changeset=835955994d5f

Carte mini-LFR: LFR-172200 dev V1.0; No série III (sans connecteurs sub-click)
Vhdl: mini-lfr_VHDLlib206 (Carte mini-LFR)
Soft: 1.0.0.2 (variante sur carte finale) = r104

Brique Brique Star-Dundee S/N 46120065.

RPW-SYS-MEB-LFR-ICD-00097 Issue2_Rev0
RPW-SYS-SSS-00013-LES + Annex_Release_Definition Issue2_rev1

History

#1 - 01/04/2014 09:47 AM - paul leroy

- Status changed from New to Resolved

fsw >= 1.0.0.5

vhdl >= 0.1.9

La fonction de gestion du temps est normalement complètement opérationnelle. Au démarrage, après un reset matériel ou simplement un redémarrage du soft, le temps local est fixé à 0x80000000 et LFR attend une séquence de synchronisation valide (TC_LFR_UPDATE_TIME + timecode).

#2 - 15/05/2014 12:11 PM - paul leroy

- Assignee changed from paul leroy to bruno katra

#3 - 13/06/2014 05:32 PM - bruno katra

- Status changed from Resolved to Closed

Le bug semble corrigé.

Grâce au mécanisme de "dummy HK", on peut voir les traces suivantes qui confirme qu'après un reset H/W on a bien le MSB à 1 :

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15:01:10.91966, TM_LFR_HK, CCSDS_VERSION_NUMBER = 0, PACKET_TYPE: TM_PACKET = 0, DATA_FIELD_HEADER_FLAG:
WITH_HEADER = 1, PROCESS_ID: RPW_PID_2 = 76, PACKET_CATEGORY: HK_ROUTINE = 4, (PACKET_ID=0xcc4),
SEGMENTATION_GROUPING_FLAG: STANDALONE_PACKET = 3, SEQUENCE_CNT=0, (PACKET_SEQUENCE_CONTROL=0xc000),
PACKET_LENGTH=117, SPARE_1=0, PUS_VERSION = 1, SPARE_2=0, SERVICE_TYPE:
HOUSEKEEPING_AND_DIAGNOSTIC_DATA_REPORTING = 3, SERVICE_SUBTYPE: HK_PARAMETER_REPORT = 25, DESTINATION_ID:
GROUND = 0, TIME=0x8000000012c2, PA_LFR_HK_REPORT_SID: LFR_HK_SID = 1, /\HK_LFR_MODE: 15, HK_LFR_DPU_SPW_ENABLED:
ENABLED = 1, /\HK_LFR_DPU_SPW_LINK_STATE: 7, /\SPARE=0x7, SY_LFR_WATCHDOG_ENABLED: ENABLED = 1,
HK_LFR_CALIB_ENABLED: ENABLED = 1, /\HK_LFR_RESET_CAUSE: 7, SY_LFR_SW_VERSION_N1=1, SY_LFR_SW_VERSION_N2=0,
SY_LFR_SW_VERSION_N3=0, SY_LFR_SW_VERSION_N4=9, SY_LFR_FPGA_VERSION_N1=0, SY_LFR_FPGA_VERSION_N2=2,
SY_LFR_FPGA_VERSION_N3=255, HK_LFR_CPU_LOAD=100.0, HK_LFR_CPU_LOAD_MAX=100.0, HK_LFR_CPU_LOAD_AVE=100.0,
HK_LFR_UPDATE_INFO_TC_CNT=65535, HK_LFR_UPDATE_TIME_TC_CNT=65535, HK_LFR_EXE_TC_CNT=65535,
HK_LFR_REJ_TC_CNT=65535, HK_LFR_LAST_EXE_TC_ID=0xffff, HK_LFR_LAST_EXE_TC_TYPE=65535,
HK_LFR_LAST_EXE_TC_SUBTYPE=65535, HK_LFR_LAST_EXE_TC_TIME=0xffffffff, HK_LFR_LAST_REJ_TC_ID=0xffff,
HK_LFR_LAST_REJ_TC_TYPE=65535, HK_LFR_LAST_REJ_TC_SUBTYPE=65535, HK_LFR_LAST_REJ_TC_TIME=0xffffffff,
HK_LFR_LE_CNT=65535, HK_LFR_ME_CNT=65535, HK_LFR_HE_CNT=65535, /\HK_LFR_LAST_ER_RID: 65535, /\HK_LFR_LAST_ER_CODE:
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255, HK_LFR_LAST_ER_TIME=0xffffffff, HK_LFR_VHDL_AA=15, HK_LFR_VHDL_SM=15, HK_LFR_VHDL_FFT=15, HK_LFR_VHDL_SR=15,
HK_LFR_VHDL_CIC=15, HK_LFR_VHDL_HK=15, HK_LFR_VHDL_IIR=15, HK_LFR_VHDL_CAL=15,
HK_LFR_DPU_SPW_PKT_RCV_CNT=65535, HK_LFR_DPU_SPW_PKT_SENT_CNT=65535, HK_LFR_DPU_SPW_TICK_OUT_CNT=255,
HK_LFR_DPU_SPW_LAST_TIMC=255, HK_LFR_LAST_FAIL_ADDR=0xffffffff, HK_LFR_TEMP_SCM=65535degC,
HK_LFR_TEMP_PCB=65535degC, HK_LFR_TEMP_FPGA=65535degC, HK_LFR_SC_V_F3=65535, HK_LFR_SC_E1_F3=65535,
HK_LFR_SC_E2_F3=65535, HK_LFR_DPU_SPW_PARITY=255, HK_LFR_DPU_SPW_DISCONNECT=255, HK_LFR_DPU_SPW_ESCAPE=255,
HK_LFR_DPU_SPW_CREDIT=255, HK_LFR_DPU_SPW_WRITE_SYNC=255, HK_LFR_DPU_SPW_RX_AHB=255,
HK_LFR_DPU_SPW_TX_AHB=255, HK_LFR_DPU_SPW_EARLY_EOP=255, HK_LFR_DPU_SPW_INVALID_ADDR=255,
HK_LFR_DPU_SPW_EEP=255, HK_LFR_DPU_SPW_RX_TOO_BIG=255, HK_LFR_TIMECODE_ERRONEOUS=255,
HK_LFR_TIMECODE_MISSING=255, HK_LFR_TIMECODE_INVALID=255, HK_LFR_TIME_TIMECODE_IT=255,
HK_LFR_TIME_NOT_SYNCHRO=255, HK_LFR_TIME_TIMECODE_CTR=255, HK_LFR_BUFFER_DPU_TC_FIFO=255,
HK_LFR_BUFFER_DPU_TM_FIFO=255, HK_LFR_AHB_CORRECTABLE=255, HK_LFR_AHB_UNCORRECTABLE=255, /\SPARE=0xff

Contexte :

Carte mini-LFR: LFR-172200 dev V1.0; No série III (sans connecteurs sub-click)

Vhdl: 0.1.16

Soft: 1.0.0.9

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