LFR-FSW - Bug #104

SY_LFR_FPGA_VERSION_N3 de TM_LFR_HK erroné

28/03/2014 02:17 PM - Gerald Saule

Status:	Closed	**Start date:**	28/03/2014
Priority:	Immediate	**Due date:**	
Assignee:	bruno katra	**% Done:**	0%
Category:		**Estimated time:**	0.00 hour
Target version:		**Spent time:**	0.00 hour
revision:	r110		

Description

TM_LFR_HK, SY_LFR_FPGA_VERSION_N3=255 est une coquille.
On attend SY_LFR_FPGA_VERSION_N3=7.

Contexte:
LPPMON Version=0.2.2 Branch=default Changeset=835955994d5f
Carte mini-LFR:LFR-172200 dev V1.0; No série III (sans connecteurs sub-click)
Vhdl: mini-lfr_0.1.7
Soft: 1.0.0.4 (variante sur carte finale)
Brique Star-Dundee S/N <blank>.

TEST CASE = s.o.

RPW-SYS-IDB-00067-LES_Issue2_Rev2
RPW-SYS-MEB-LFR-ICD-00097 Issue2_Rev2
RPW-SYS-SSS-00013-LES + Annex_Release_Definition Issue2_rev2

History

#1 - 31/03/2014 08:17 AM - paul leroy

- Status changed from New to Resolved

fsw >= 1.0.0.5
bug identifié et corrigé

#2 - 11/06/2014 01:55 PM - bruno katra

- Status changed from Resolved to Feedback

- Assignee set to paul leroy

- Priority changed from Normal to Immediate

le bug avait disparu en fsw 1.0.0.7 :

Traces HK avec vhdl 0.1.16 :

16:45:20.550404, TM_LFR_HK, CCSDS_VERSION_NUMBER = 0, PACKET_TYPE: TM_PACKET = 0, DATA_FIELD_HEADER_FLAG: WITH_HEADER = 1, PROCESS_ID: RPW_PID_2 = 76, PACKET_CATEGORY: HK_ROUTINE = 4, (PACKET_ID=0xcc4), SEGMENTATION_GROUPING_FLAG: STANDALONE_PACKET = 3, SEQUENCE_CNT=1, (PACKET_SEQUENCE_CONTROL=0xc001), PACKET_LENGTH=117, SPARE_1=0, PUS_VERSION = 1, SPARE_2=0, SERVICE_TYPE: HOUSEKEEPING_AND_DIAGNOSTIC_DATA_REPORTING = 3, SERVICE_SUBTYPE: HK_PARAMETER_REPORT = 25, DESTINATION_ID: GROUND = 0, TIME=0x800000022833, PA_LFR_HK_REPORT_SID: LFR_HK_SID = 1, HK_LFR_MODE: STANDBY = 0, HK_LFR_DPU_SPW_ENABLED: ENABLED = 1, HK_LFR_DPU_SPW_LINK_STATE: RUN = 5, SPARE=0x0, SY_LFR_WATCHDOG_ENABLED: DISABLED = 0, HK_LFR_CALIB_ENABLED: DISABLED = 0, HK_LFR_RESET_CAUSE: UNKNOWN_CAUSE = 0, **SY_LFR_SW_VERSION_N1=1, SY_LFR_SW_VERSION_N2=0, SY_LFR_SW_VERSION_N3=0, SY_LFR_SW_VERSION_N4=7, SY_LFR_FPGA_VERSION_N1=0, SY_LFR_FPGA_VERSION_N2=1, SY_LFR_FPGA_VERSION_N3=16**, HK_LFR_CPU_LOAD=1.56862745098, HK_LFR_CPU_LOAD_MAX=1.56862745098, HK_LFR_CPU_LOAD_AVE=0.0, HK_LFR_UPDATE_INFO_TC_CNT=0, HK_LFR_UPDATE_TIME_TC_CNT=0, HK_LFR_EXE_TC_CNT=0, HK_LFR_REJ_TC_CNT=0, HK_LFR_LAST_EXE_TC_ID=0x0, HK_LFR_LAST_EXE_TC_TYPE=0, HK_LFR_LAST_EXE_TC_SUBTYPE=0, HK_LFR_LAST_EXE_TC_TIME=0x000000000000, HK_LFR_LAST_REJ_TC_ID=0x0, HK_LFR_LAST_REJ_TC_TYPE=0, HK_LFR_LAST_REJ_TC_SUBTYPE=0, HK_LFR_LAST_REJ_TC_TIME=0x000000000000, HK_LFR_LE_CNT=0, HK_LFR_ME_CNT=0, HK_LFR_HE_CNT=0, HK_LFR_LAST_ER_RID: NO_ERROR = 0, HK_LFR_LAST_ER_CODE: NO_ERROR = 0, HK_LFR_LAST_ER_TIME=0x000000000000, HK_LFR_VHDL_AA=0, HK_LFR_VHDL_SM=0, HK_LFR_VHDL_FFT=0, HK_LFR_VHDL_SR=0, HK_LFR_VHDL_CIC=0, HK_LFR_VHDL_HK=0, HK_LFR_VHDL_IIR=0, HK_LFR_VHDL_CAL=0, HK_LFR_DPU_SPW_PKT_RCV_CNT=0, HK_LFR_DPU_SPW_PKT_SENT_CNT=1,

HK_LFR_DPU_SPW_TICK_OUT_CNT=0, HK_LFR_DPU_SPW_LAST_TIMC=0, HK_LFR_LAST_FAIL_ADDR=0x0, HK_LFR_TEMP_SCM=0degC, HK_LFR_TEMP_PCB=0degC, HK_LFR_TEMP_FPGA=0degC, HK_LFR_SC_V_F3=0, HK_LFR_SC_E1_F3=0, HK_LFR_SC_E2_F3=0, HK_LFR_DPU_SPW_PARITY=0, HK_LFR_DPU_SPW_DISCONNECT=0, HK_LFR_DPU_SPW_ESCAPE=0, HK_LFR_DPU_SPW_CREDIT=0, HK_LFR_DPU_SPW_WRITE_SYNC=0, HK_LFR_DPU_SPW_RX_AHB=0, HK_LFR_DPU_SPW_TX_AHB=0, HK_LFR_DPU_SPW_EARLY_EOP=0, HK_LFR_DPU_SPW_INVALID_ADDR=0, HK_LFR_DPU_SPW_EEP=0, HK_LFR_DPU_SPW_RX_TOO_BIG=0, HK_LFR_TIMECODE_ERRONEOUS=0, HK_LFR_TIMECODE_MISSING=0, HK_LFR_TIMECODE_INVALID=0, HK_LFR_TIME_TIMECODE_IT=0, HK_LFR_TIME_NOT_SYNCHRO=0, HK_LFR_TIME_TIMECODE_CTR=0, HK_LFR_BUFFER_DPU_TC_FIFO=0, HK_LFR_BUFFER_DPU_TM_FIFO=0, HK_LFR_AHB_CORRECTABLE=0, HK_LFR_AHB_UNCORRECTABLE=0, SPARE=0x0

Traces HK avec vhdl 0.1.9 :

09:45:59.920493, TM_LFR_HK, CCSDS_VERSION_NUMBER = 0, PACKET_TYPE: TM_PACKET = 0, DATA_FIELD_HEADER_FLAG: WITH_HEADER = 1, PROCESS_ID: RPW_PID_2 = 76, PACKET_CATEGORY: HK_ROUTINE = 4, (PACKET_ID=0xcc4), SEGMENTATION_GROUPING_FLAG: STANDALONE_PACKET = 3, SEQUENCE_CNT=1, (PACKET_SEQUENCE_CONTROL=0xc001), PACKET_LENGTH=117, SPARE_1=0, PUS_VERSION = 1, SPARE_2=0, SERVICE_TYPE: HOUSEKEEPING_AND_DIAGNOSTIC_DATA_REPORTING = 3, SERVICE_SUBTYPE: HK_PARAMETER_REPORT = 25, DESTINATION_ID: GROUND = 0, TIME=0x800000024241, PA_LFR_HK_REPORT_SID: LFR_HK_SID = 1, HK_LFR_MODE: NORMAL = 1, HK_LFR_DPU_SPW_ENABLED: ENABLED = 1, HK_LFR_DPU_SPW_LINK_STATE: RUN = 5, SPARE=0x0, SY_LFR_WATCHDOG_ENABLED: DISABLED = 0, HK_LFR_CALIB_ENABLED: DISABLED = 0, HK_LFR_RESET_CAUSE: UNKNOWN_CAUSE = 0, **SY_LFR_SW_VERSION_N1=1, SY_LFR_SW_VERSION_N2=0, SY_LFR_SW_VERSION_N3=0, SY_LFR_SW_VERSION_N4=7, SY_LFR_FPGA_VERSION_N1=0, SY_LFR_FPGA_VERSION_N2=1, SY_LFR_FPGA_VERSION_N3=9,** HK_LFR_CPU_LOAD=14.9019607843, HK_LFR_CPU_LOAD_MAX=14.9019607843, HK_LFR_CPU_LOAD_AVE=0.0, HK_LFR_UPDATE_INFO_TC_CNT=0, HK_LFR_UPDATE_TIME_TC_CNT=0, HK_LFR_EXE_TC_CNT=1, HK_LFR_REJ_TC_CNT=0, HK_LFR_LAST_EXE_TC_ID=0x1ccc, HK_LFR_LAST_EXE_TC_TYPE=181, HK_LFR_LAST_EXE_TC_SUBTYPE=41, HK_LFR_LAST_EXE_TC_TIME=0x800000008f97, HK_LFR_LAST_REJ_TC_ID=0x0, HK_LFR_LAST_REJ_TC_TYPE=0, HK_LFR_LAST_REJ_TC_SUBTYPE=0, HK_LFR_LAST_REJ_TC_TIME=0x000000000000, HK_LFR_LE_CNT=0, HK_LFR_ME_CNT=0, HK_LFR_HE_CNT=0, HK_LFR_LAST_ER_RID: NO_ERROR = 0, HK_LFR_LAST_ER_CODE: NO_ERROR = 0, HK_LFR_LAST_ER_TIME=0x000000000000, HK_LFR_VHDL_AA=0, HK_LFR_VHDL_SM=0, HK_LFR_VHDL_FFT=0, HK_LFR_VHDL_SR=0, HK_LFR_VHDL_CIC=0, HK_LFR_VHDL_HK=0, HK_LFR_VHDL_IIR=0, HK_LFR_VHDL_CAL=0, HK_LFR_DPU_SPW_PKT_RCV_CNT=1, HK_LFR_DPU_SPW_PKT_SENT_CNT=2, HK_LFR_DPU_SPW_TICK_OUT_CNT=0, HK_LFR_DPU_SPW_LAST_TIMC=0, HK_LFR_LAST_FAIL_ADDR=0x0, HK_LFR_TEMP_SCM=0degC, HK_LFR_TEMP_PCB=0degC, HK_LFR_TEMP_FPGA=0degC, HK_LFR_SC_V_F3=65098, HK_LFR_SC_E1_F3=65076, HK_LFR_SC_E2_F3=65078, HK_LFR_DPU_SPW_PARITY=0, HK_LFR_DPU_SPW_DISCONNECT=0, HK_LFR_DPU_SPW_ESCAPE=0, HK_LFR_DPU_SPW_CREDIT=0, HK_LFR_DPU_SPW_WRITE_SYNC=0, HK_LFR_DPU_SPW_RX_AHB=0, HK_LFR_DPU_SPW_TX_AHB=0, HK_LFR_DPU_SPW_EARLY_EOP=0, HK_LFR_DPU_SPW_INVALID_ADDR=0, HK_LFR_DPU_SPW_EEP=0, HK_LFR_DPU_SPW_RX_TOO_BIG=0, HK_LFR_TIMECODE_ERRONEOUS=0, HK_LFR_TIMECODE_MISSING=0, HK_LFR_TIMECODE_INVALID=0, HK_LFR_TIME_TIMECODE_IT=0, HK_LFR_TIME_NOT_SYNCHRO=0, HK_LFR_TIME_TIMECODE_CTR=0, HK_LFR_BUFFER_DPU_TC_FIFO=0, HK_LFR_BUFFER_DPU_TM_FIFO=0, HK_LFR_AHB_CORRECTABLE=0, HK_LFR_AHB_UNCORRECTABLE=0, SPARE=0x0

LE BUG EST REAPPARU EN FSW 1.0.0.8 :

SY_LFR_FPGA_VERSION_N3=255

traces avec vhdl 0.1.16 :

11:34:56.14916, TM_LFR_HK, CCSDS_VERSION_NUMBER = 0, PACKET_TYPE: TM_PACKET = 0, DATA_FIELD_HEADER_FLAG: WITH_HEADER = 1, PROCESS_ID: RPW_PID_2 = 76, PACKET_CATEGORY: HK_ROUTINE = 4, (PACKET_ID=0xcc4), SEGMENTATION_GROUPING_FLAG: STANDALONE_PACKET = 3, SEQUENCE_CNT=1, (PACKET_SEQUENCE_CONTROL=0xc001), PACKET_LENGTH=117, SPARE_1=0, PUS_VERSION = 1, SPARE_2=0, SERVICE_TYPE: HOUSEKEEPING_AND_DIAGNOSTIC_DATA_REPORTING = 3, SERVICE_SUBTYPE: HK_PARAMETER_REPORT = 25, DESTINATION_ID: GROUND = 0, TIME=0x8000000241ff, PA_LFR_HK_REPORT_SID: LFR_HK_SID = 1, HK_LFR_MODE: NORMAL = 1, HK_LFR_DPU_SPW_ENABLED: ENABLED = 1, HK_LFR_DPU_SPW_LINK_STATE: RUN = 5, SPARE=0x0, SY_LFR_WATCHDOG_ENABLED: DISABLED = 0, HK_LFR_CALIB_ENABLED: DISABLED = 0, HK_LFR_RESET_CAUSE: UNKNOWN_CAUSE = 0, **SY_LFR_SW_VERSION_N1=1, SY_LFR_SW_VERSION_N2=0, SY_LFR_SW_VERSION_N3=0, SY_LFR_SW_VERSION_N4=8, SY_LFR_FPGA_VERSION_N1=0, SY_LFR_FPGA_VERSION_N2=2, SY_LFR_FPGA_VERSION_N3=255,** HK_LFR_CPU_LOAD=14.5098039216, HK_LFR_CPU_LOAD_MAX=14.5098039216, HK_LFR_CPU_LOAD_AVE=0.0, HK_LFR_UPDATE_INFO_TC_CNT=0, HK_LFR_UPDATE_TIME_TC_CNT=0, HK_LFR_EXE_TC_CNT=1, HK_LFR_REJ_TC_CNT=0, HK_LFR_LAST_EXE_TC_ID=0x1ccc, HK_LFR_LAST_EXE_TC_TYPE=181, HK_LFR_LAST_EXE_TC_SUBTYPE=41, HK_LFR_LAST_EXE_TC_TIME=0x800000008f4e, HK_LFR_LAST_REJ_TC_ID=0x0, HK_LFR_LAST_REJ_TC_TYPE=0, HK_LFR_LAST_REJ_TC_SUBTYPE=0, HK_LFR_LAST_REJ_TC_TIME=0x000000000000, HK_LFR_LE_CNT=0, HK_LFR_ME_CNT=0, HK_LFR_HE_CNT=0, HK_LFR_LAST_ER_RID: NO_ERROR = 0, HK_LFR_LAST_ER_CODE: NO_ERROR = 0, HK_LFR_LAST_ER_TIME=0x000000000000, HK_LFR_VHDL_AA=0, HK_LFR_VHDL_SM=0, HK_LFR_VHDL_FFT=0, HK_LFR_VHDL_SR=0, HK_LFR_VHDL_CIC=0, HK_LFR_VHDL_HK=0, HK_LFR_VHDL_IIR=0, HK_LFR_VHDL_CAL=0, HK_LFR_DPU_SPW_PKT_RCV_CNT=1, HK_LFR_DPU_SPW_PKT_SENT_CNT=2, HK_LFR_DPU_SPW_TICK_OUT_CNT=0, HK_LFR_DPU_SPW_LAST_TIMC=0, HK_LFR_LAST_FAIL_ADDR=0x0, HK_LFR_TEMP_SCM=0degC, HK_LFR_TEMP_PCB=0degC, HK_LFR_TEMP_FPGA=0degC, HK_LFR_SC_V_F3=58297, HK_LFR_SC_E1_F3=58263, HK_LFR_SC_E2_F3=58312, HK_LFR_DPU_SPW_PARITY=0, HK_LFR_DPU_SPW_DISCONNECT=0, HK_LFR_DPU_SPW_ESCAPE=0, HK_LFR_DPU_SPW_CREDIT=0, HK_LFR_DPU_SPW_WRITE_SYNC=0, HK_LFR_DPU_SPW_RX_AHB=0, HK_LFR_DPU_SPW_TX_AHB=0, HK_LFR_DPU_SPW_EARLY_EOP=0, HK_LFR_DPU_SPW_INVALID_ADDR=0, HK_LFR_DPU_SPW_EEP=0, HK_LFR_DPU_SPW_RX_TOO_BIG=0, HK_LFR_TIMECODE_ERRONEOUS=0, HK_LFR_TIMECODE_MISSING=0, HK_LFR_TIMECODE_INVALID=0, HK_LFR_TIME_TIMECODE_IT=0, HK_LFR_TIME_NOT_SYNCHRO=0, HK_LFR_TIME_TIMECODE_CTR=0, HK_LFR_BUFFER_DPU_TC_FIFO=0, HK_LFR_BUFFER_DPU_TM_FIFO=0, HK_LFR_AHB_CORRECTABLE=0, HK_LFR_AHB_UNCORRECTABLE=0, SPARE=0x0

Contexte:
LPPMON: Version=0.2.2 Branch=default Changeset=835955994d5f
Carte mini-LFR: LFR-172200 dev V1.0; No série III (sans connecteurs sub-click)
Vhdl: mini-lfr_0.1.9 et 0.1.16
Brique Star-Dundee S/N 46120065.
Soft:1.0.0.7 et 1.0.0.8 (variante sur carte finale)

#3 - 12/06/2014 08:24 AM - paul leroy

- Status changed from Feedback to Resolved

- Assignee changed from paul leroy to bruno katra

fsw >= 1.0.0.9

bug identifié et corrigé. la vesrion du VHDL s'affiche maintenant également dans le message initial envoyé sur le port série pendant le boot

#4 - 13/06/2014 05:36 PM - bruno katra

- Status changed from Resolved to Closed

Retesté en 1.0.0.9 : bug corrigé

15:01:17.829798, TM_LFR_HK, CCSDS_VERSION_NUMBER = 0, PACKET_TYPE: TM_PACKET = 0, DATA_FIELD_HEADER_FLAG: WITH_HEADER = 1, PROCESS_ID: RPW_PID_2 = 76, PACKET_CATEGORY: HK_ROUTINE = 4, (PACKET_ID=0xcc4), SEGMENTATION_GROUPING_FLAG: STANDALONE_PACKET = 3, SEQUENCE_CNT=0, (PACKET_SEQUENCE_CONTROL=0xc000), PACKET_LENGTH=117, SPARE_1=0, PUS_VERSION = 1, SPARE_2=0, SERVICE_TYPE: HOUSEKEEPING_AND_DIAGNOSTIC_DATA_REPORTING = 3, SERVICE_SUBTYPE: HK_PARAMETER_REPORT = 25, DESTINATION_ID: GROUND = 0, TIME=0x800000072ab5, PA_LFR_HK_REPORT_SID: LFR_HK_SID = 1, HK_LFR_MODE: STANDBY = 0, HK_LFR_DPU_SPW_ENABLED: ENABLED = 1, HK_LFR_DPU_SPW_LINK_STATE: RUN = 5, SPARE=0x0, SY_LFR_WATCHDOG_ENABLED: DISABLED = 0, HK_LFR_CALIB_ENABLED: DISABLED = 0, HK_LFR_RESET_CAUSE: UNKNOWN_CAUSE = 0, SY_LFR_SW_VERSION_N1=1, SY_LFR_SW_VERSION_N2=0, SY_LFR_SW_VERSION_N3=0, SY_LFR_SW_VERSION_N4=9, **SY_LFR_FPGA_VERSION_N1=0, SY_LFR_FPGA_VERSION_N2=1, SY_LFR_FPGA_VERSION_N3=16**