

Issues

#	Project	Tracker	Status	Priority	Subject	Assignee	Updated
14	Solar Orbiter LFR	Task	Closed	High	Fichier de configuration FPGA	Jean-Christophe Pellion	13/03/2014 07:17 AM
46	VHDLlib	Task	Closed	Normal	WFP Validation	Jean-Christophe Pellion	02/12/2016 01:15 PM
45	VHDLlib	Task	Closed	Normal	WFP - fault detection	Jean-Christophe Pellion	02/12/2016 01:13 PM
555	Solar Orbiter LFR	Task	Closed	Normal	Errata RPW-MEB-LFR-SPC-00061-1-8_FPGA_Architecture_Design	Jean-Christophe Pellion	26/10/2015 04:20 PM
412	VHDLlib	Feature	Closed	Normal	Fenêtrage	Jean-Christophe Pellion	22/10/2015 10:40 AM
258	Solar Orbiter LFR	Support	Closed	Normal	Numéro de version du code VHDL	Jean-Christophe Pellion	10/02/2015 04:27 PM
227	Solar Orbiter LFR	Task	Closed	Normal	Calibration	Jean-Christophe Pellion	10/02/2015 04:22 PM
93	VHDLlib	Bug	Closed	Normal	versionner les fichiers vhdlib.txt, vhdsim.txt	Jean-Christophe Pellion	07/01/2015 02:43 PM
234	Solar Orbiter LFR	Bug	Closed	Normal	Problème sur la forme d'onde ("écrêtage" vers 1.5 V d'amplitudes)	Jean-Christophe Pellion	02/10/2014 09:26 AM
242	VHDLlib	Feature	Closed	Normal	créer des fichiers de contrainte d'horloge pour MINI-LFR et EM	Jean-Christophe Pellion	25/09/2014 05:45 PM
33	Solar Orbiter LFR	Feature	Closed	Normal	sous-échantillonnage des signaux électriques DC (s1, s2 et s3)	Jean-Christophe Pellion	03/09/2014 09:42 AM
31	Solar Orbiter LFR	Feature	Closed	Normal	filtrage + sous échantillonnage 8 voies	Jean-Christophe Pellion	03/09/2014 09:42 AM
13	Solar Orbiter LFR	Task	Closed	Normal	Mise à jour de la documentation VHDL	Jean-Christophe Pellion	13/03/2014 07:17 AM
6	VHDLlib	Bug	Closed	Normal	écriture des données snapshot f0 f1 f2 erronée	Jean-Christophe Pellion	25/02/2014 02:16 PM
10	VHDLlib	Task	Closed	Normal	LFR EM Bitsream - 0.0.6 - Validation	Jean-Christophe Pellion	23/01/2014 01:50 PM
5	VHDLlib	Bug	Closed	Normal	IRQ from WaveFormPicker	Jean-Christophe Pellion	19/11/2013 09:42 AM
44	VHDLlib	Task	Rejected	Normal	WaveFormPicker Caracterisation	Jean-Christophe Pellion	02/12/2016 01:14 PM
96	VHDLlib	Bug	Rejected	Normal	DMA latency to access External memory	Jean-Christophe Pellion	02/12/2016 01:10 PM