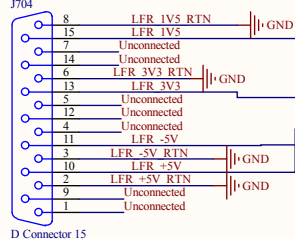
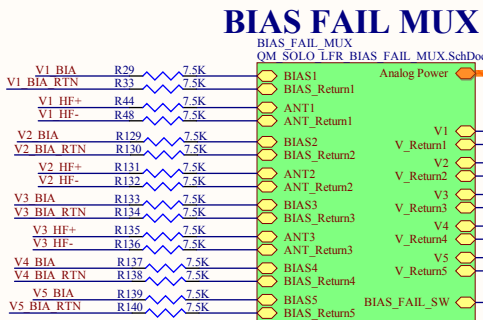
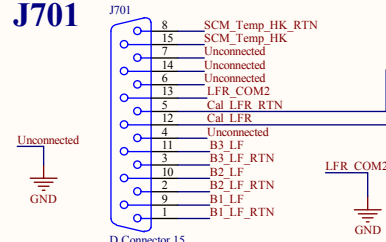


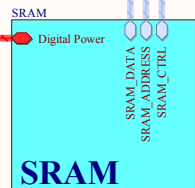
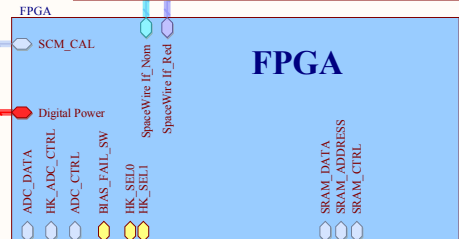
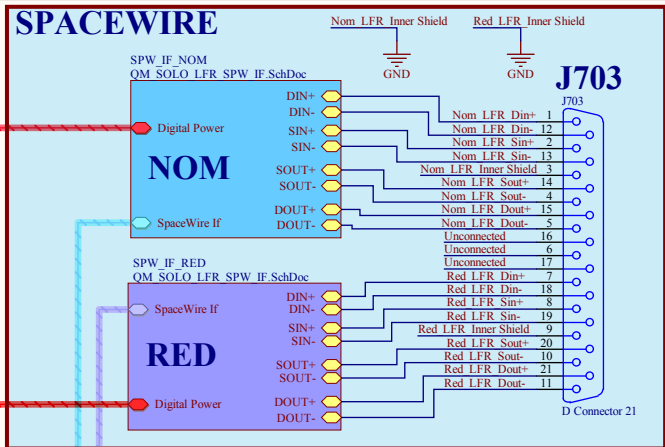
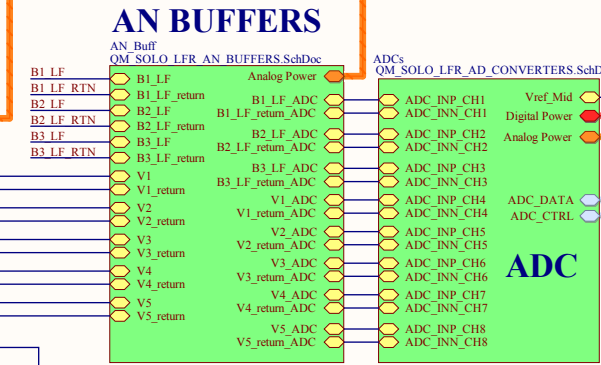
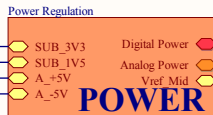
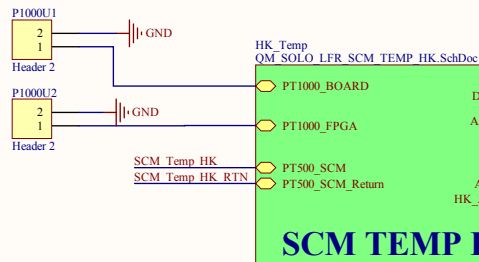
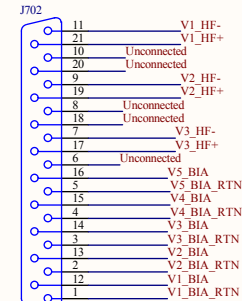
J704



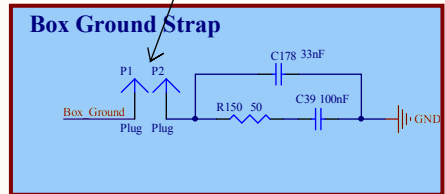
J701



J702



Need discussion with Vincent



CHANGELOG
QM_CHANGELOG.SchDoc

Title	LFR_QM_TOP	Author	Alexis Jeandet	
Size	A3	Number	LFR-172200-FM	
Date	13/10/2014	Time	14:58:44	
Contact	alexis.jeandet@lpp.polytechnique.fr	Revision	01.07	
File	F:\Missions\Satellites\SolarOrbiter\LFR\PCB\QM\QM_SOLO_LFR_TOP.SchDoc			

CHANGELOG

09/04/2014

- Moved analog input buffers resistors before the swithes.
- C21 (100nF cap @ SUB1.5V input) footprint changed to 0805.
- Connected SENS input for RHFL4913 to Vout.
- 2.5V analogic connected to sub 3.3V.
- added R/C Slow start on 2.5V RHFL4913.
- 1.8V MSK5822 VBias input moved from 5V to sub 3.3V.

14/04/2014

- Connected SCM cal and SPW shield to GND.
- Unconnected Pin are connected to Unconnected Net which is tied to GND.

15/04/2014

- Updated ground strap, it's now removable and the circuit is a R C//R.

22/04/2014

- Connected 3.3V regulator VBIAS input to sub 3.3V.
- Connected MSKs Latch input to GND.
- Connected RHFL4913 INH inputs to GND.
- Replaced DG419 with 54HC4053 for bais/ant mux.

24/04/2014

- Replaced EM SRAM with FM SRAM UT8ER1M32.

25/04/2014

- Replaced DG419 with 54HC4053 for HK mux.
- Replaced DG419 with 54HC4053 for SCM CAL mux.
- Replaced DAC reference with qualified one.

30/04/2014

- Replaced EM Oscillators with FM.
- Replaced EM HK DAC with FM.

05/05/2014

- Added SPW enable signal.
- Replaced LT1009 by RH1009.
- Replaced MSK 3.3V regulator by RHFL4913.
- Added filtering structures on +/-5V.
- Added RC reset circuit for FPGA.
- Changed 400k resistors on ADC bias to 2x200k.

06/05/2014

- Changed power input inductors from 100µH to 10µH.

16/05/2014

- Updated footprints from Vincent observations.

30/06/2014

- added reset connection on FPGA(mistake on 05/05/2014).
- Grounding strap update.
- Replaced _ by U in components names and mutlisheet generator rules.

15/07/2014



- added missing decoupling capacitors on ADC sheet

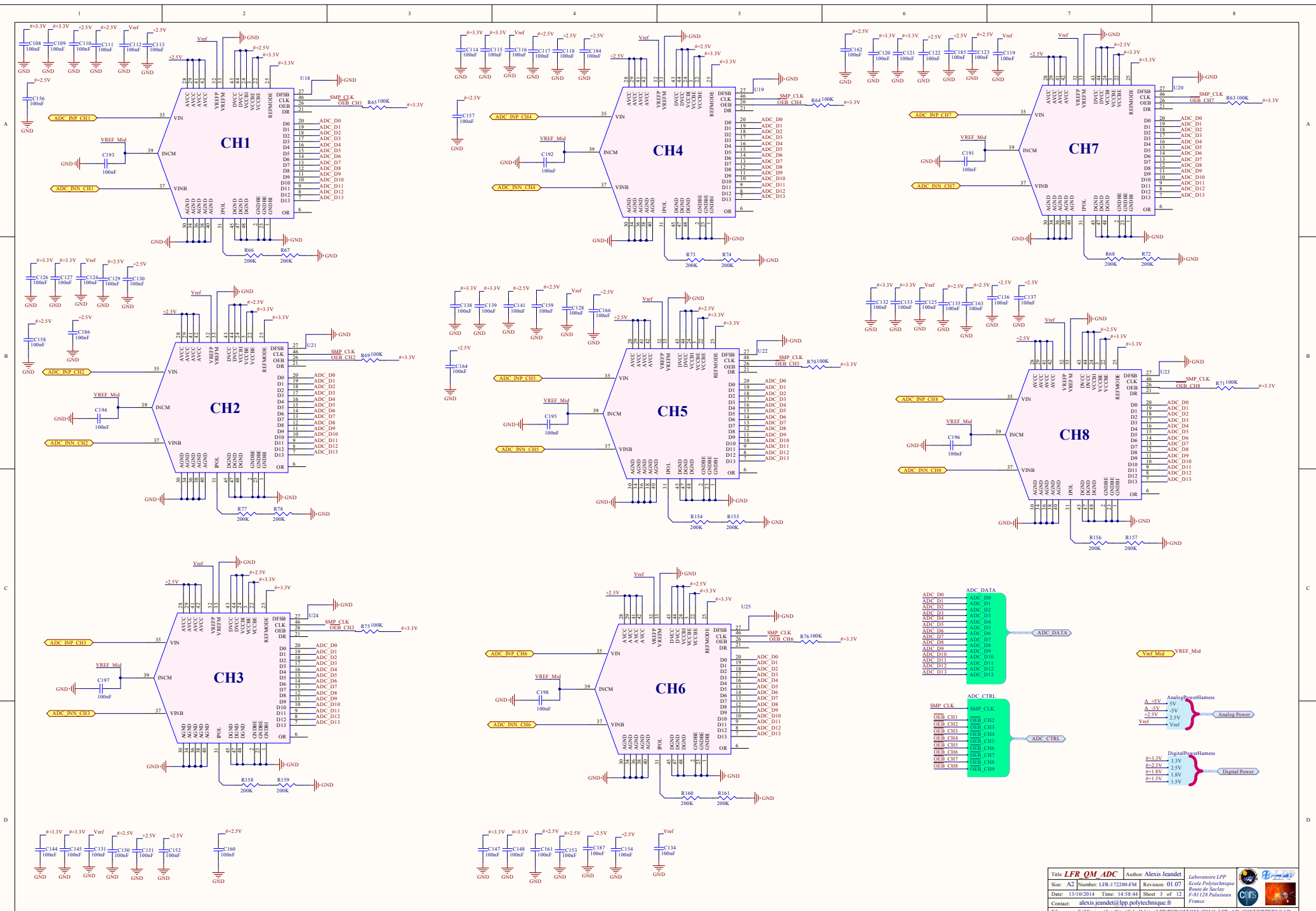
13/08/2014

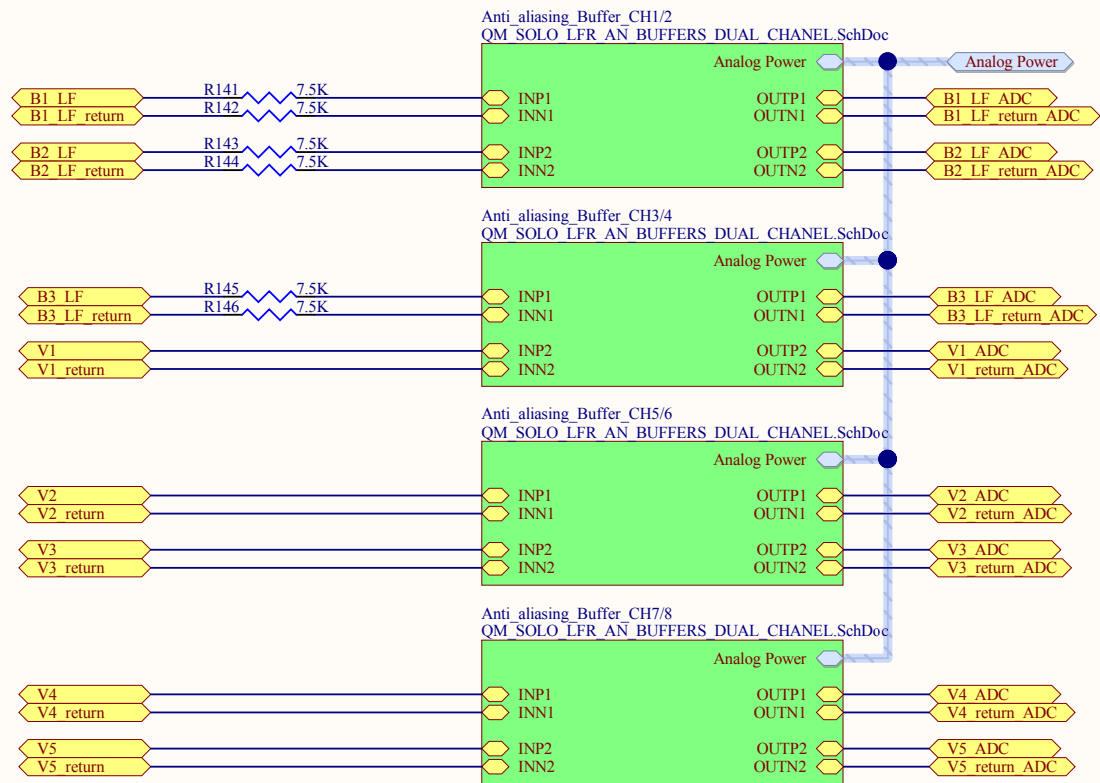
- Updated FPGA connections from steel netlist

12/10/2014

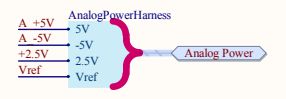
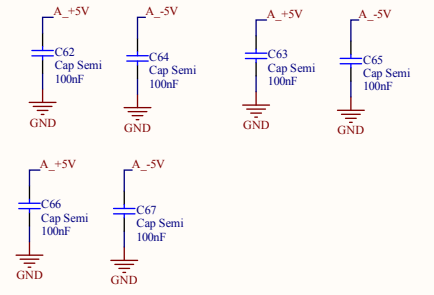
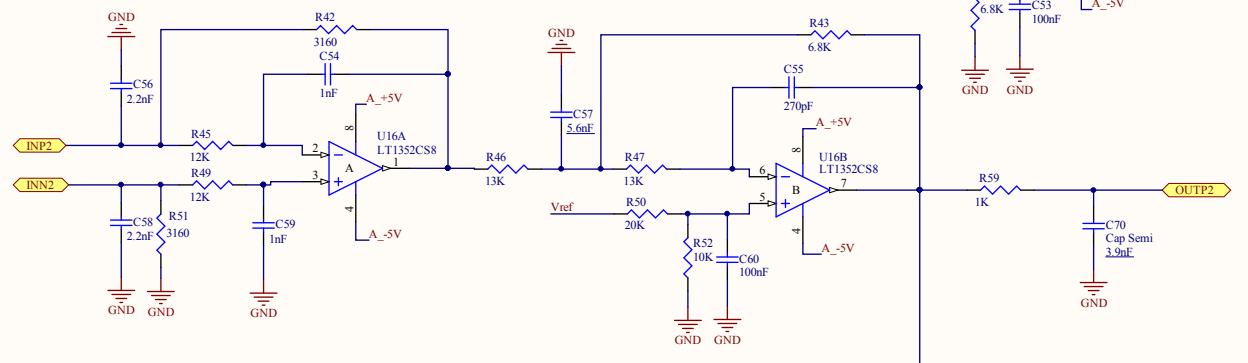
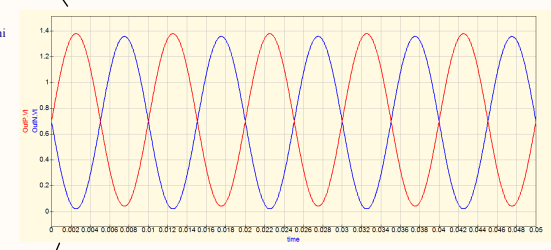
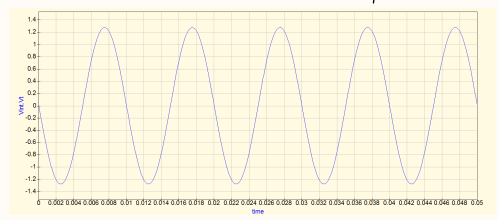
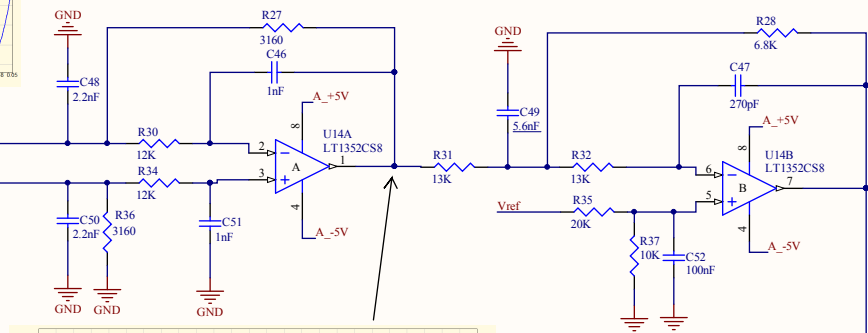
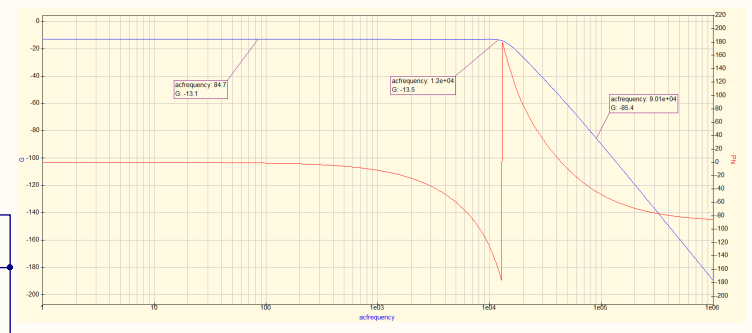
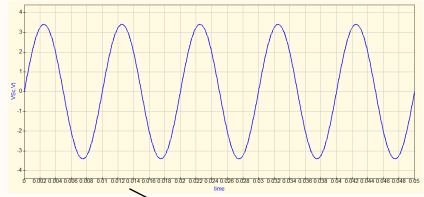
- Added RHFACT541K01V level shifter
- Vref/2 buffered by U39B(OPAMP)
- Added simple resistive voltage divider to reduce ADC's clk input to 2.5V

Title CHANGELOG		Author: Alexis Jeandet		  Laboratoire LPP Ecole Polytechnique Route de Saclay F-91128 Palaiseau France
Size: A4	Number: LFR-172200-FM	Revision: 01.07		
Date: 13/10/2014	Time: 14:58:44	Sheet 2 of 12		
Contact: alexis.jeandet@lpp.polytechnique.fr				
File: F:\Missions\Satellites\SolarOrbiter\LFR\PCB\QM\QM_CHANGELOG.SchDoc				



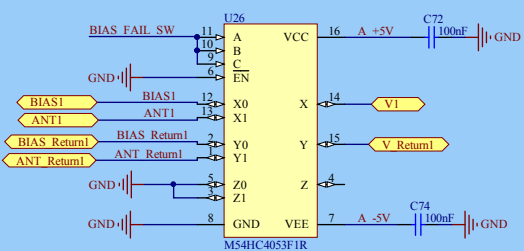


Title LFR_QM_AN		Author: Alexis Jeandet		
Size: A4	Number: LFR-172200-FM	Revision: 01.07		
Date: 13/10/2014	Time: 14:58:44	Sheet 4 of 12		
Contact: alexis.jeandet@lpp.polytechnique.fr				
File: F:\Missions\Satellites\SolarOrbiter\LFR\PCB\QM\QM_SOLO_LFR_AN_BUFFERS.SchDoc				

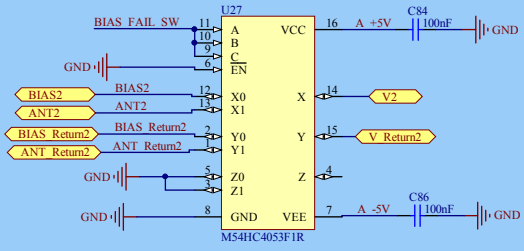


Title	LFR_QM_BUFF	Author:	Alexis Jeandet	Laboratoire LPP Ecole Polytechnique Route de Saclay F-91128 Palaiseau France
Size:	A3	Number:	LFR-172200-FM	
Date:	13/10/2014	Time:	14:58:45	
Contact:	alexis.jeandet@lpp.polytechnique.fr	Sheet	5 of 12	
File:	F:\Missions\Satellites\SolarOrbiter\LFR\PCB\QM\SOLO_LFR_AN_BUFFERS_DUAL_CHANL.SchDoc			

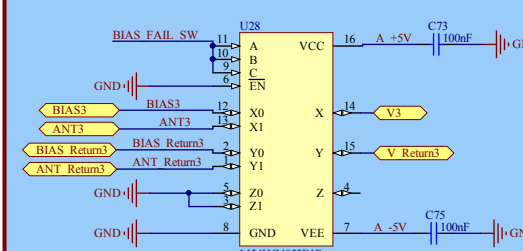
BIAS1/ANT1 Channel



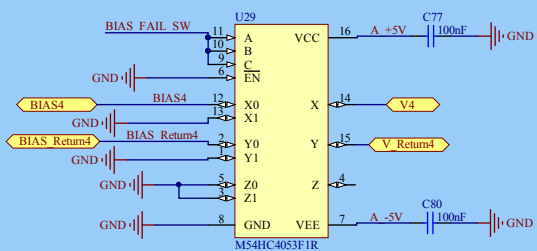
BIAS2/ANT2 Channel



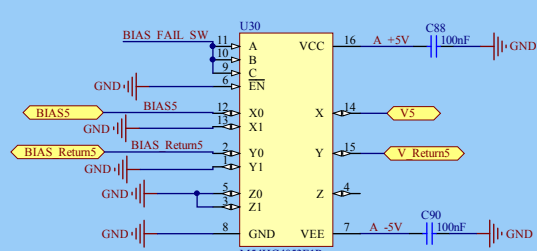
BIAS3/ANT3 Channel



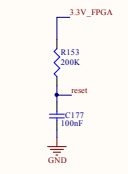
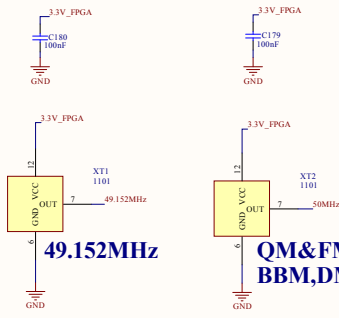
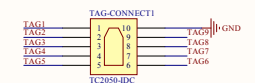
BIAS4 Channel



BIAS5 Channel



TAG-Probe



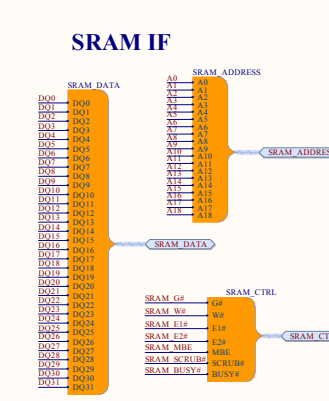
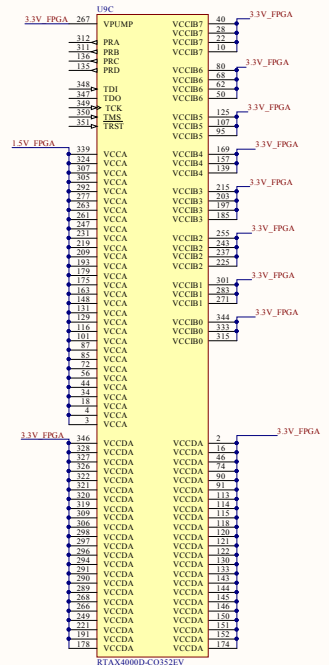
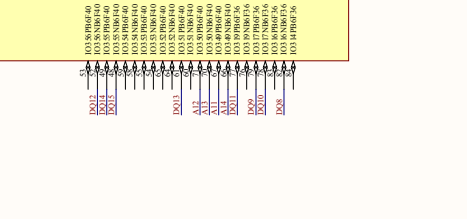
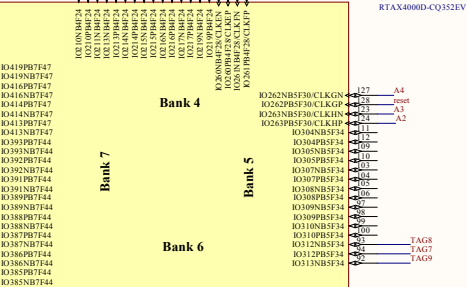
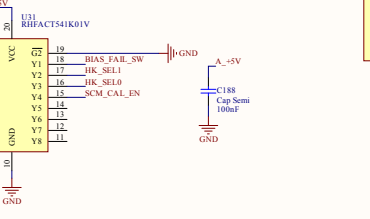
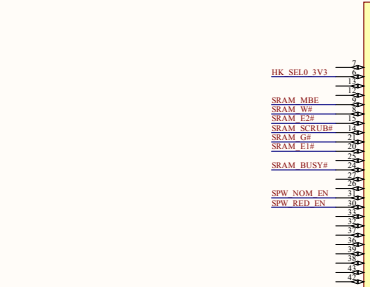
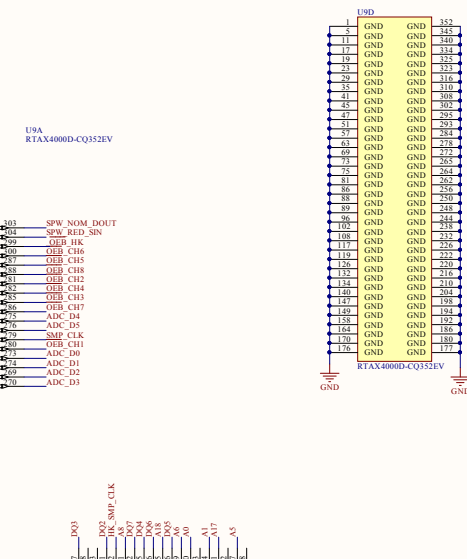
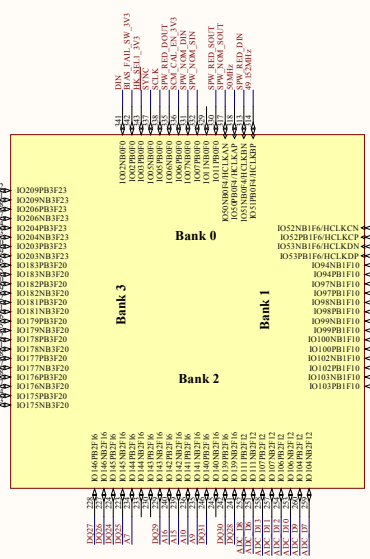
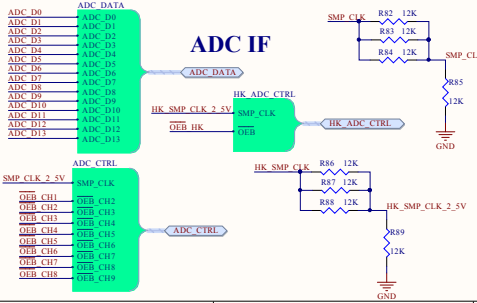
SPW Nominal Link



SPW Redundant Link



ADC IF



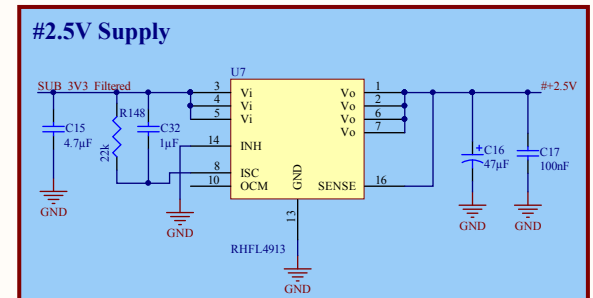
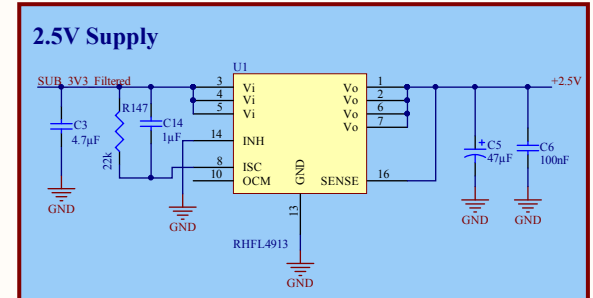
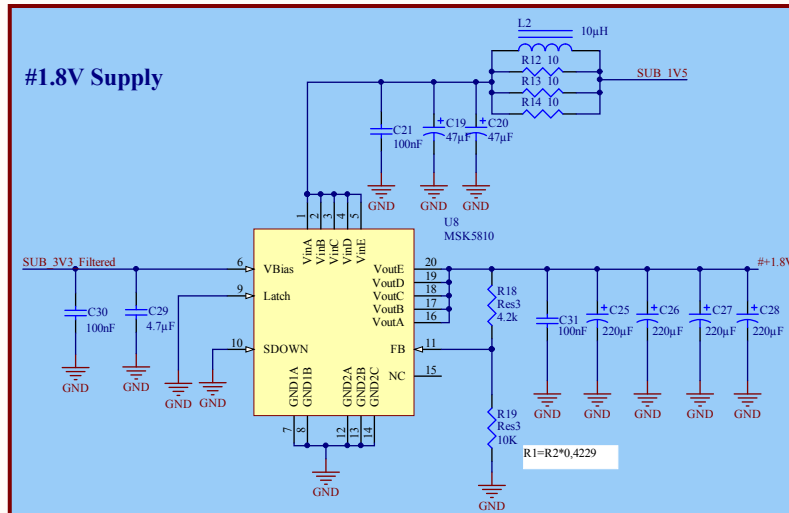
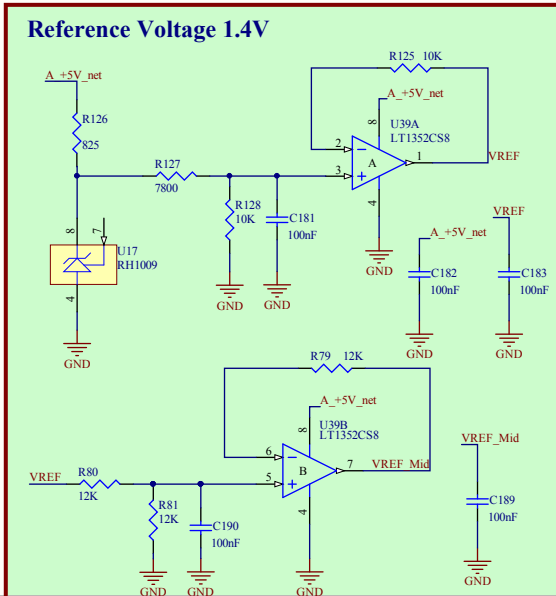
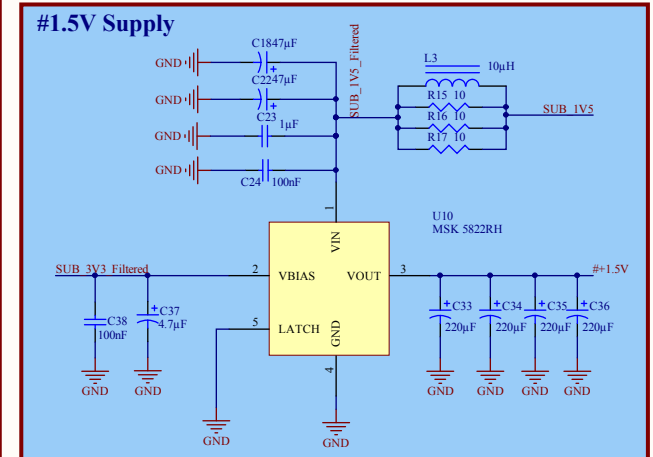
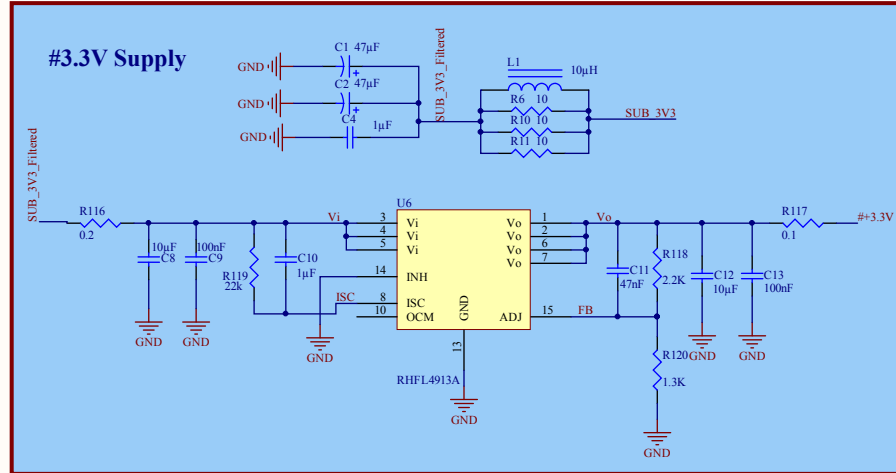
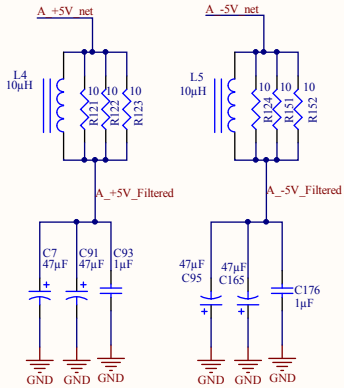
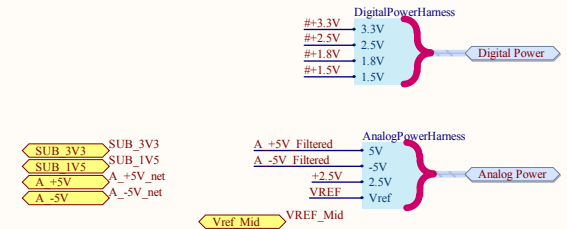
Characterization

Power-Up Characterization

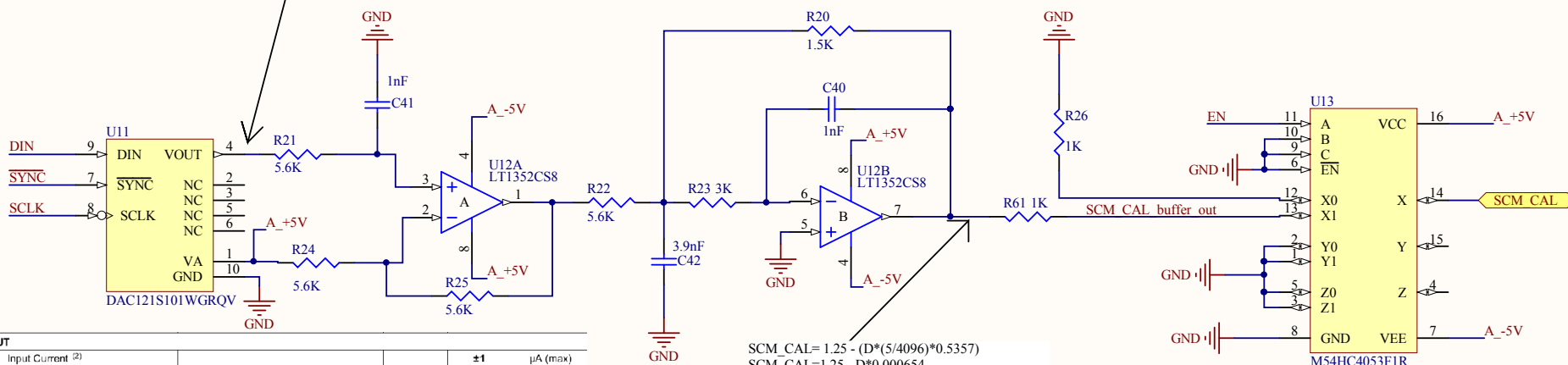
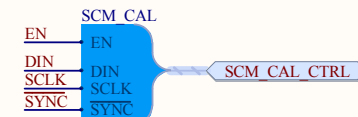
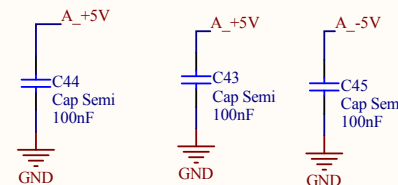
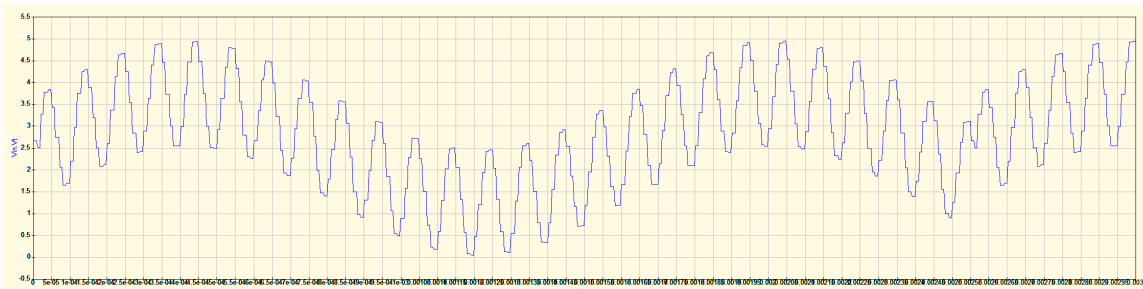
Power supplies for the RTAX-S/SL devices can power up in any sequence. Figure 1 and Figure 2 show the power-up characteristics for the different sequencing between VCCA (1.5 V) and VCCDA/VCCIBx (3.3 V). No significant transient current (>5 mA) is observed with either sequence.

Uses Rev H for MSK5822 and MSK5810 regulators documentation!

220uF => TAZ-H package
 47uF => TAZ-H package
 4.7uF => TAJ-B package

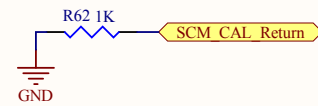
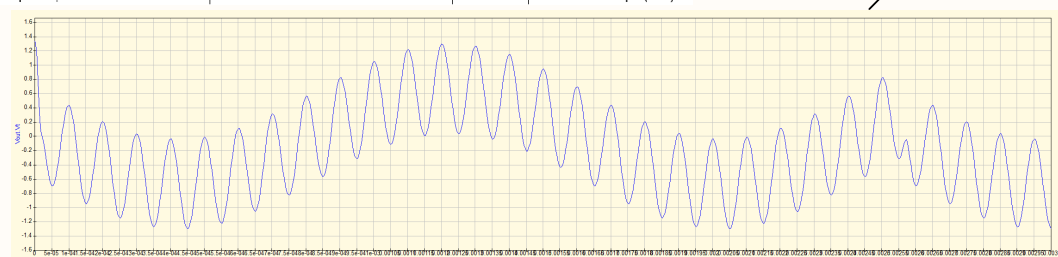


REQ-RPW-LFR-4706 LFR shall deliver a calibration signal to the SCM. This signal will be the sum of two sinus waves, at different frequencies $f_1 = 625$ Hz and $f_2 = 10$ kHz, with amplitudes of 500 mVpp, a sampling frequency of [TBD], a resolution of 8 bits and a duration of 4 s.
 When not used, the calibration signal will be tied to ground (TBC) via an analog switch.

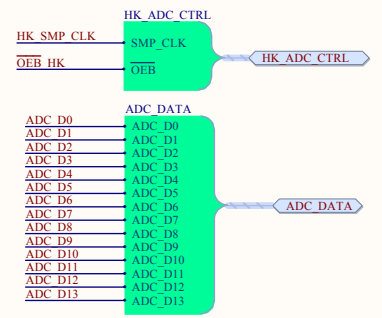
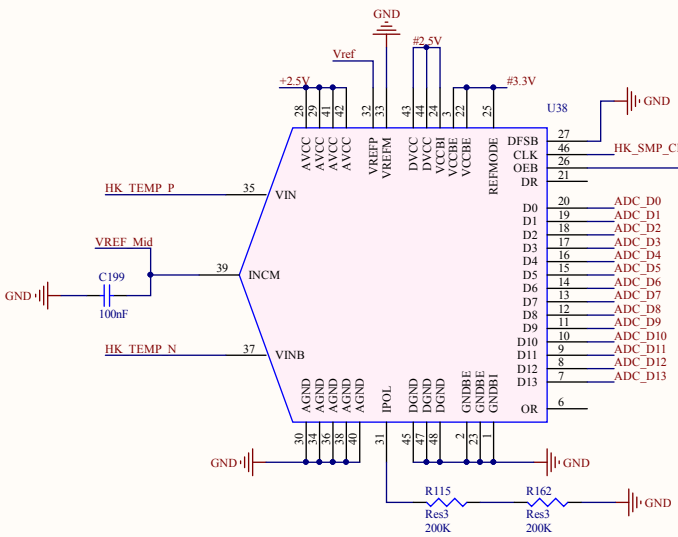
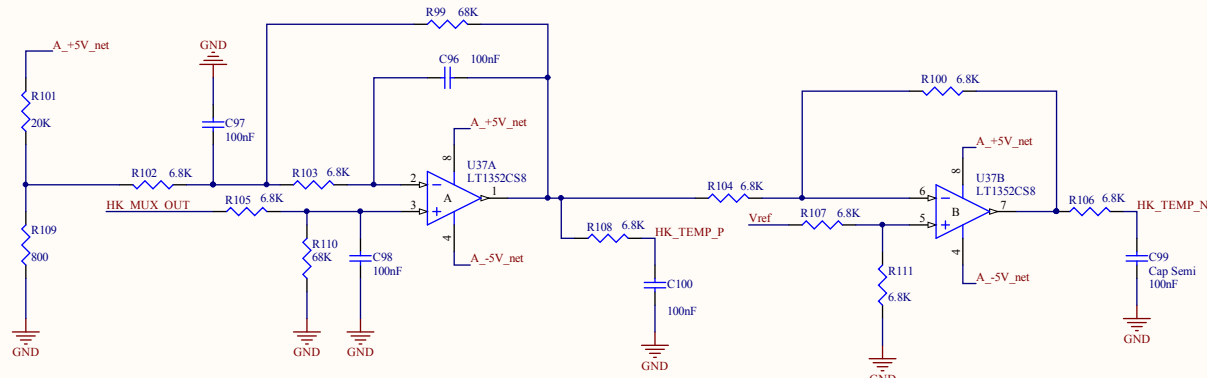
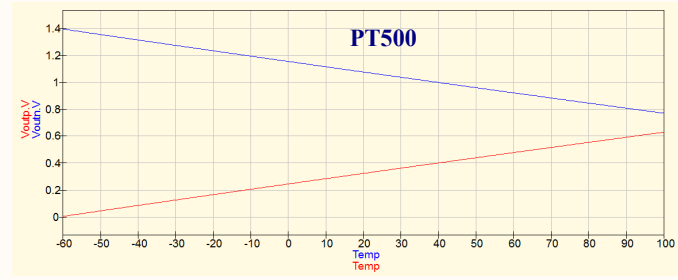
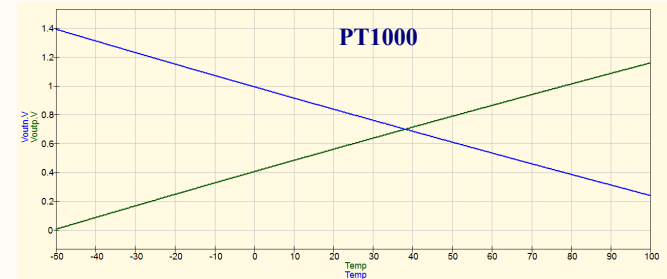
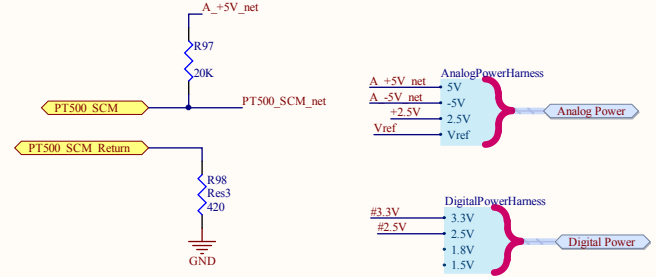
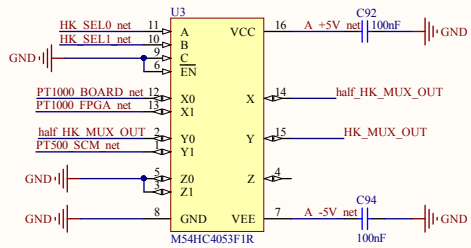
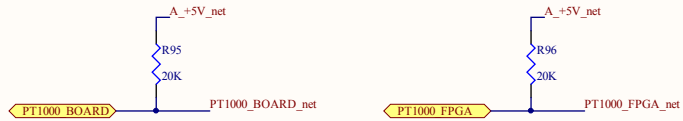


$$SCM_CAL = 1.25 - (D * (5/4096) * 0.5357)$$

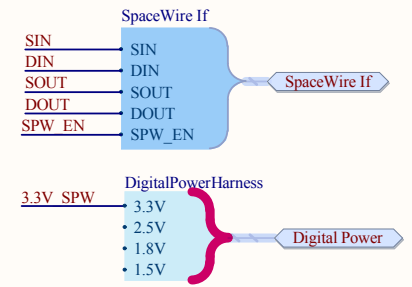
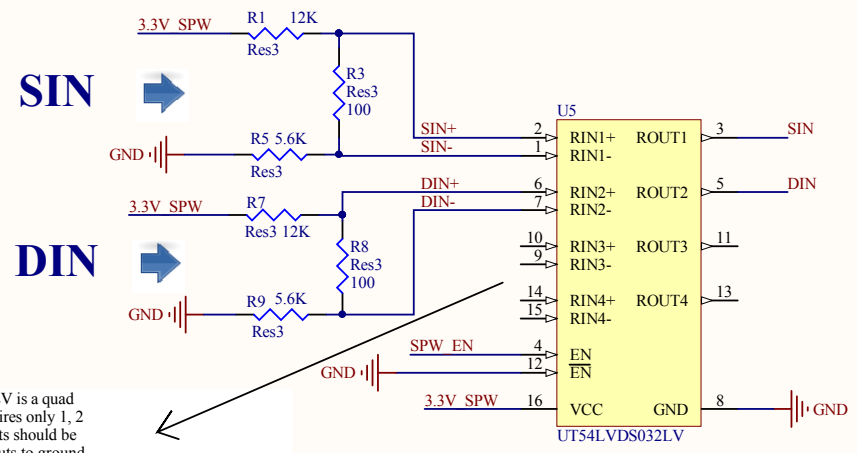
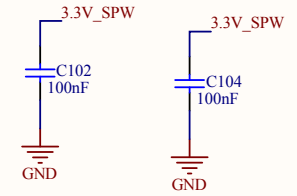
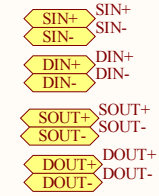
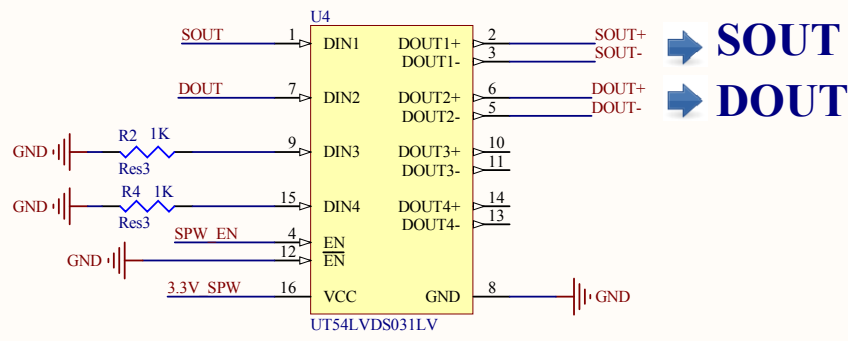
$$SCM_CAL = 1.25 - D * 0.000654$$



Title	LFR_QM_CAL	Author:	Alexis Jeandet	
Size:	A4	Number:	LFR-172200-FM	
Date:	13/10/2014	Time:	14:58:45	
Contact:	alexis.jeandet@lpp.polytechnique.fr			
File:	F:\Missions\Satellites\SolarOrbiter\LFR\PCB\QM\QM_SOLO_LFR_SCM_CAL.SchDoc			



Title	LFR_QM_HK	Author	Alexis Jeandet	
Size	A3	Number	LFR-172200-FM	
Date	13/10/2014	Time	14:58:45	
Contact	alexis.jeandet@lpp.polytechnique.fr		Sheet 10 of 12	
File	F:\Missions\Satellites\SolarOrbiter\LFR\PCB\QM\SOLO_LFR_SCM_TEMP_HK_SchDoc			

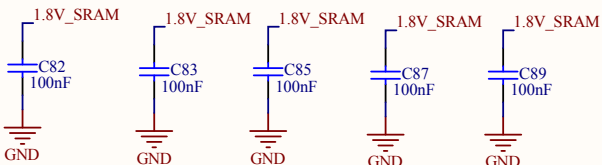
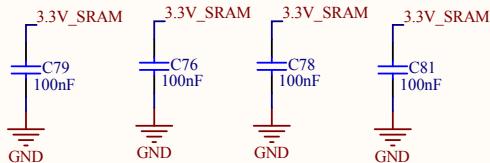
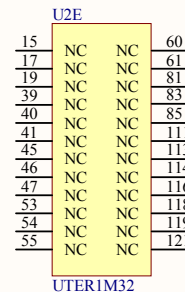
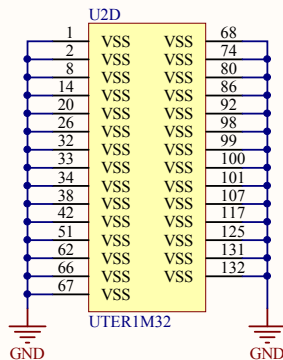
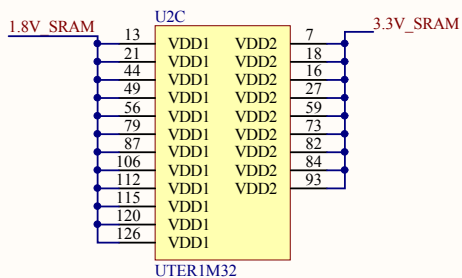
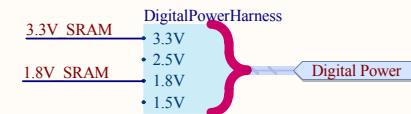
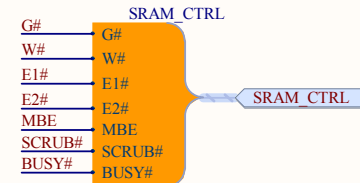
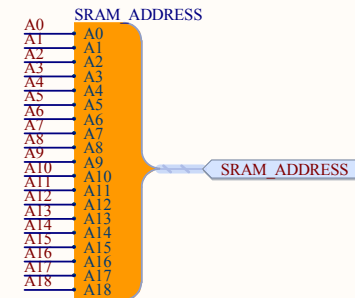
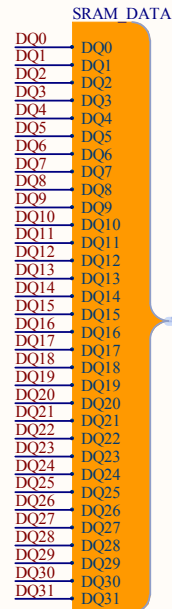
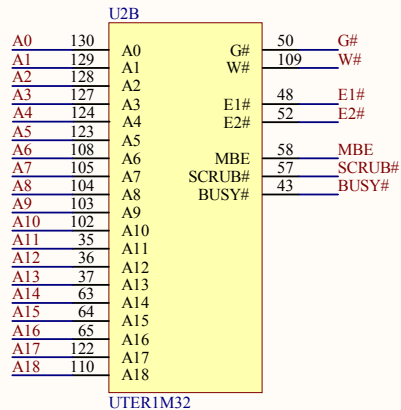
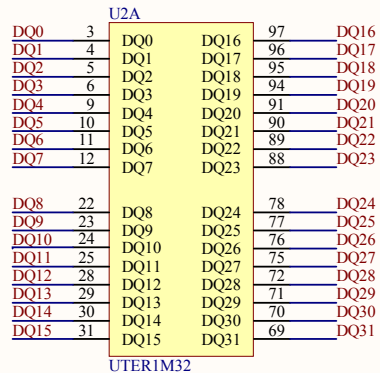



1. Open Input Pins. The UT54LVDS032LV is a quad receiver device, and if an application requires only 1, 2 or 3 receivers, the unused channel(s) inputs should be left OPEN. Do not tie unused receiver inputs to ground or any other voltages. The input is biased by internal high value pull up and pull down resistors to set the output to a HIGH state. This internal circuitry will guarantee a HIGH, stable output state for open inputs.

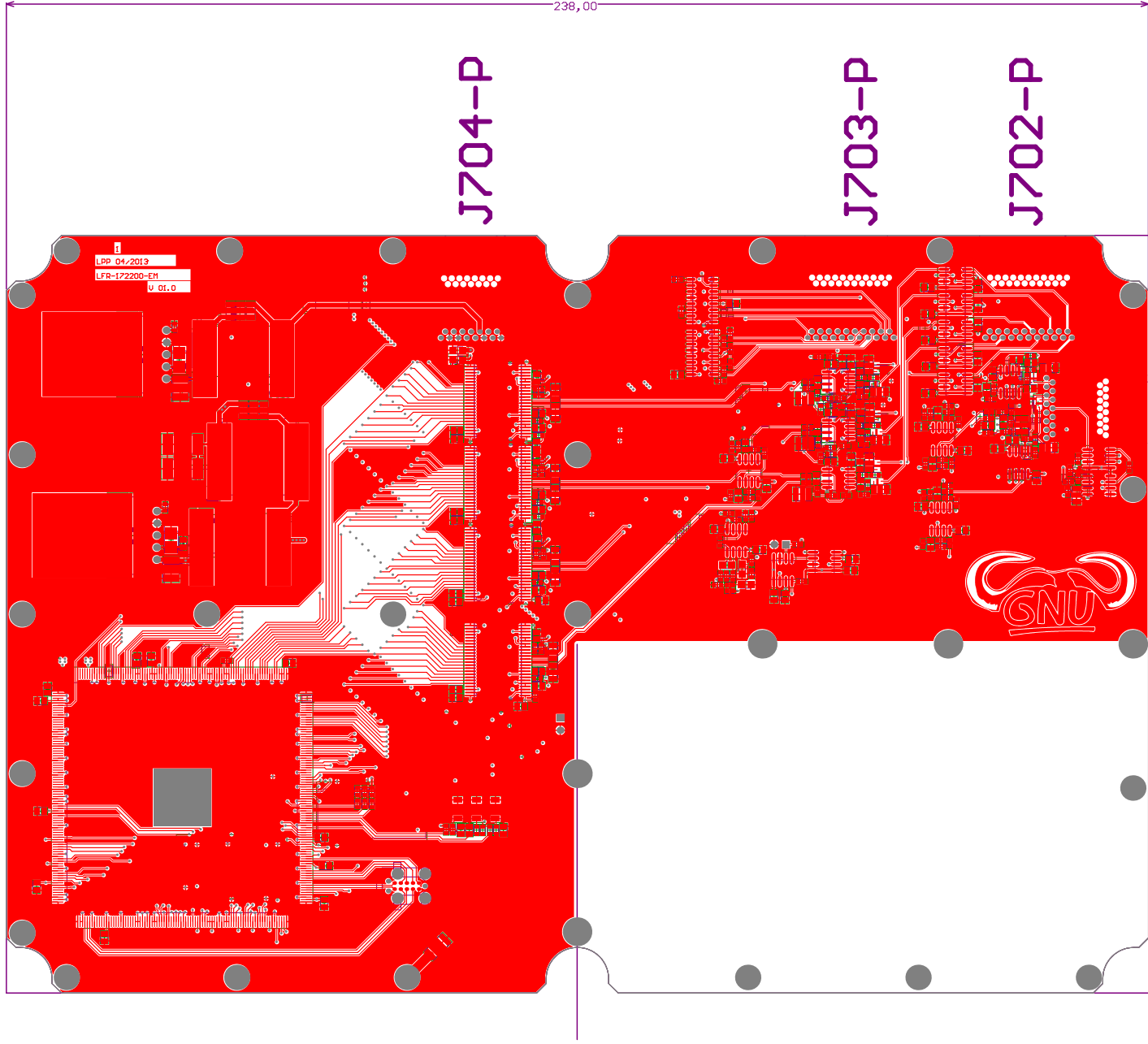
cf : <http://www.aeroflex.com/ams/pagesproduct/datasheets/LVDSReceiver3v.pdf>

Title LFR_QM_SPW		Author: Alexis Jeandet	
Size: A4	Number: LFR-172200-FM	Revision: 01.07	
Date: 13/10/2014	Time: 14:58:45	Sheet 11 of 12	
Contact: alexis.jeandet@lpp.polytechnique.fr			
File: F:\Missions\Satellites\SolarOrbiter\LFR\PCB\QM\QM_SOLO_LFR_SPW_IF.SchDoc			





Title	LFR_QM_SRAM	Author:	Alexis Jeandet	
Size:	A4	Number:	LFR-172200-FM	
Date:	13/10/2014	Time:	14:58:45	
Contact:	alexis.jeandet@lpp.polytechnique.fr			
File:	F:\Missions\Satellites\SolarOrbiter\LFR\PCB\QM\QM_SOLO_LFR_SRAM.SchDoc			



238,00

J704-P

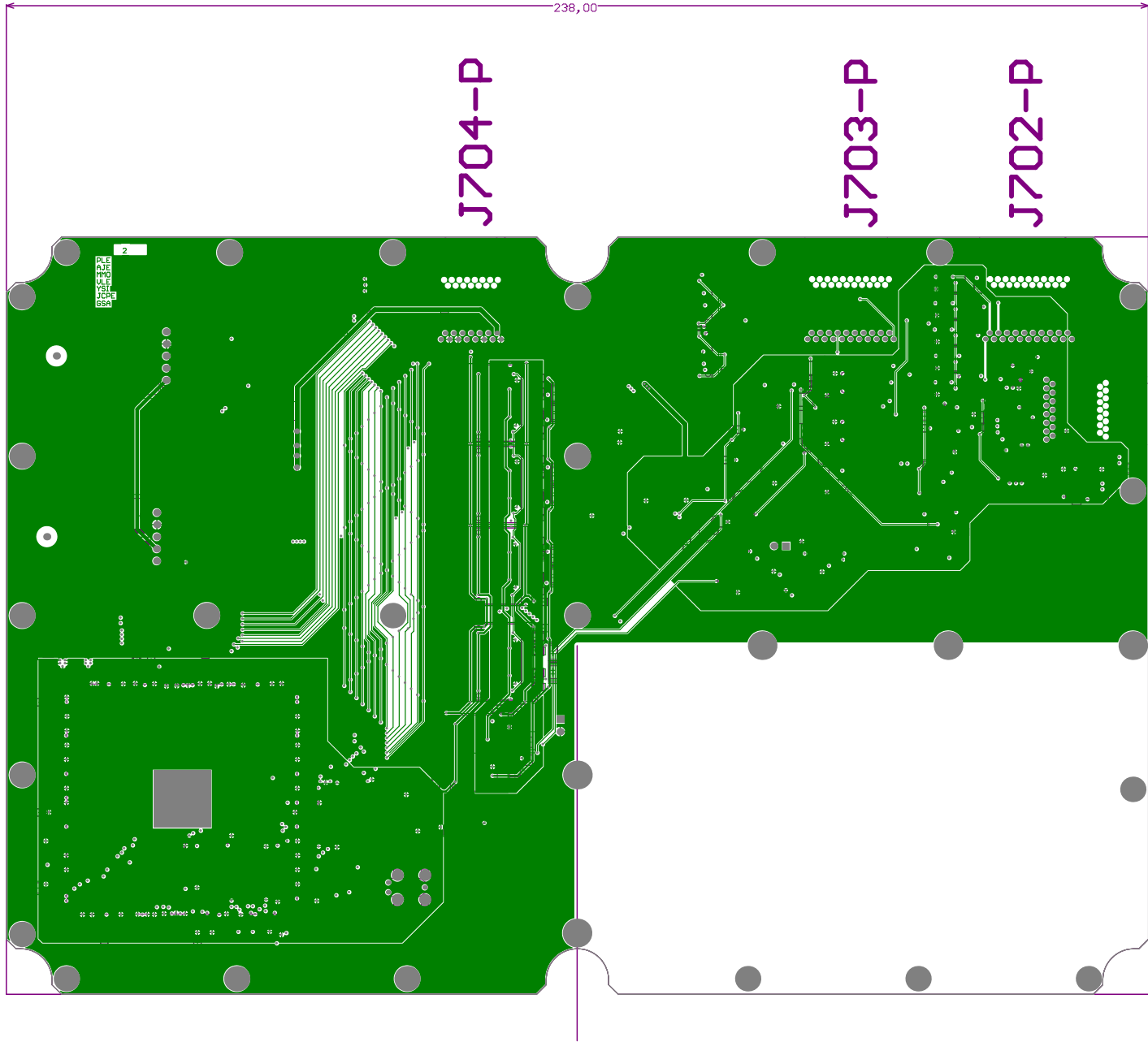
J703-P

J702-P

J701-P
B_LF/MF

158,00





J704-P

J703-P

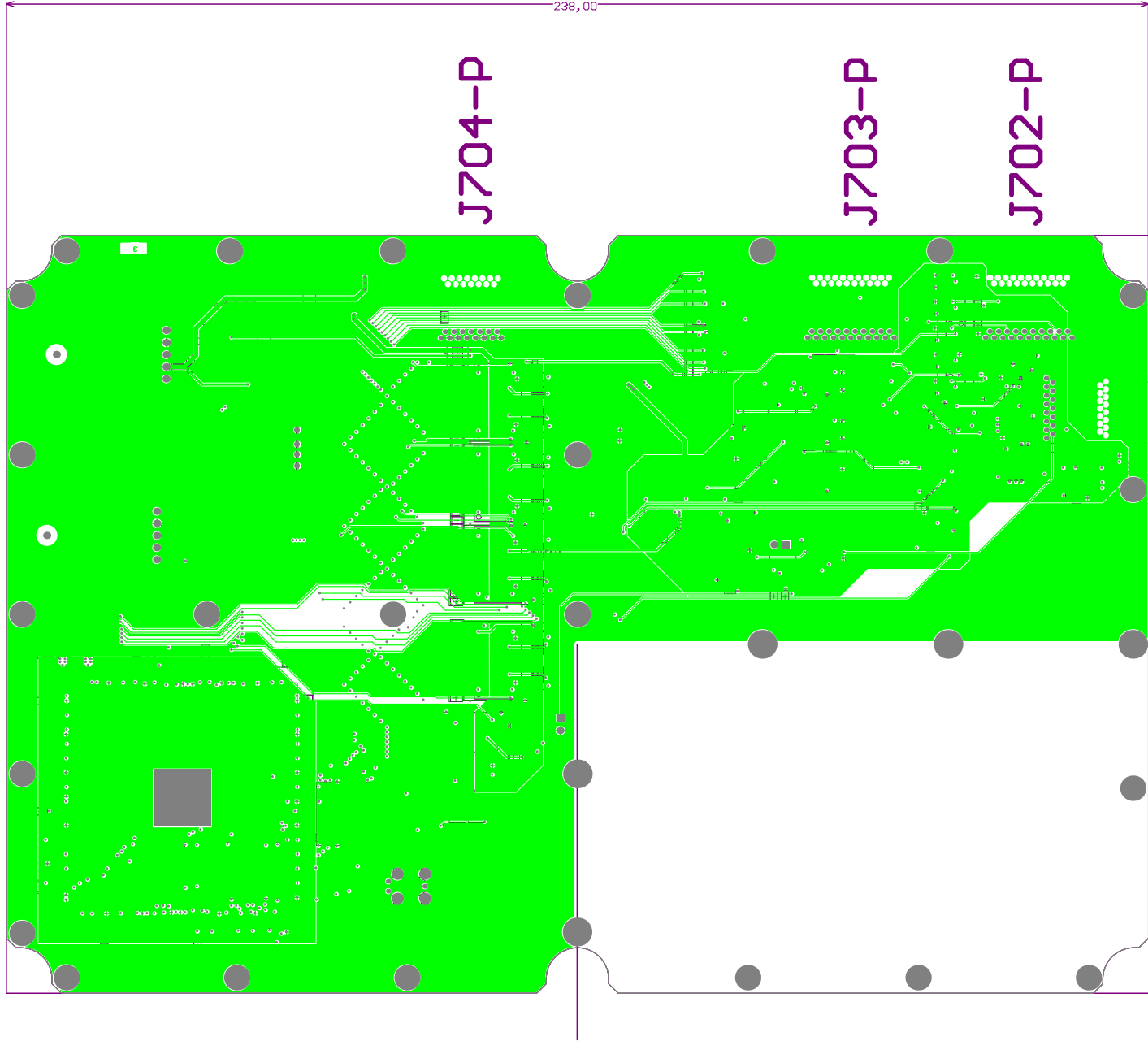
J702-P

J701-P
B_LF/MF

158,00

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J704-P

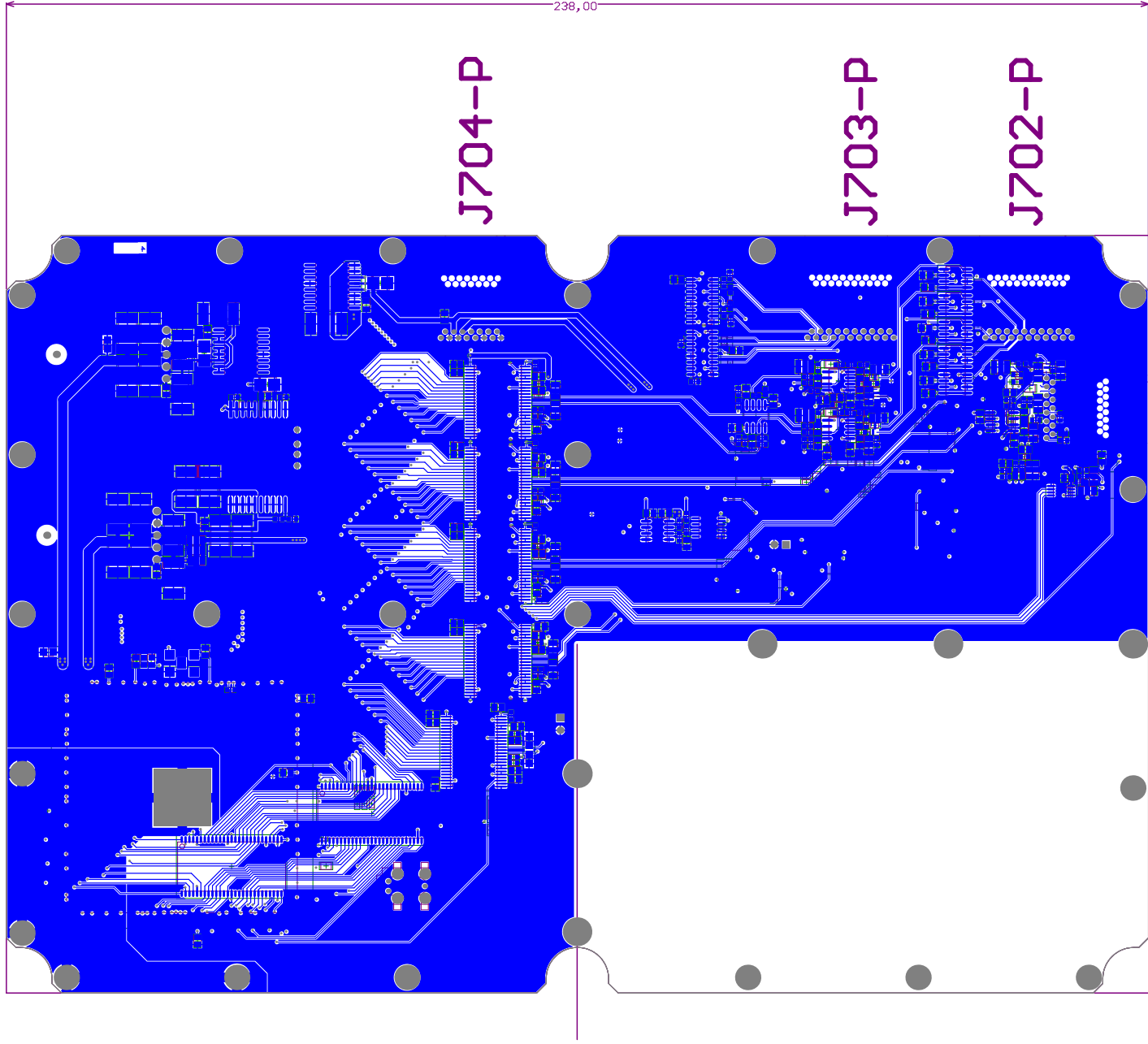
J703-P

J702-P

J701-P
B_LF/MF

158,00





J704-P

J703-P

J702-P

J701-P
B_LF/MF

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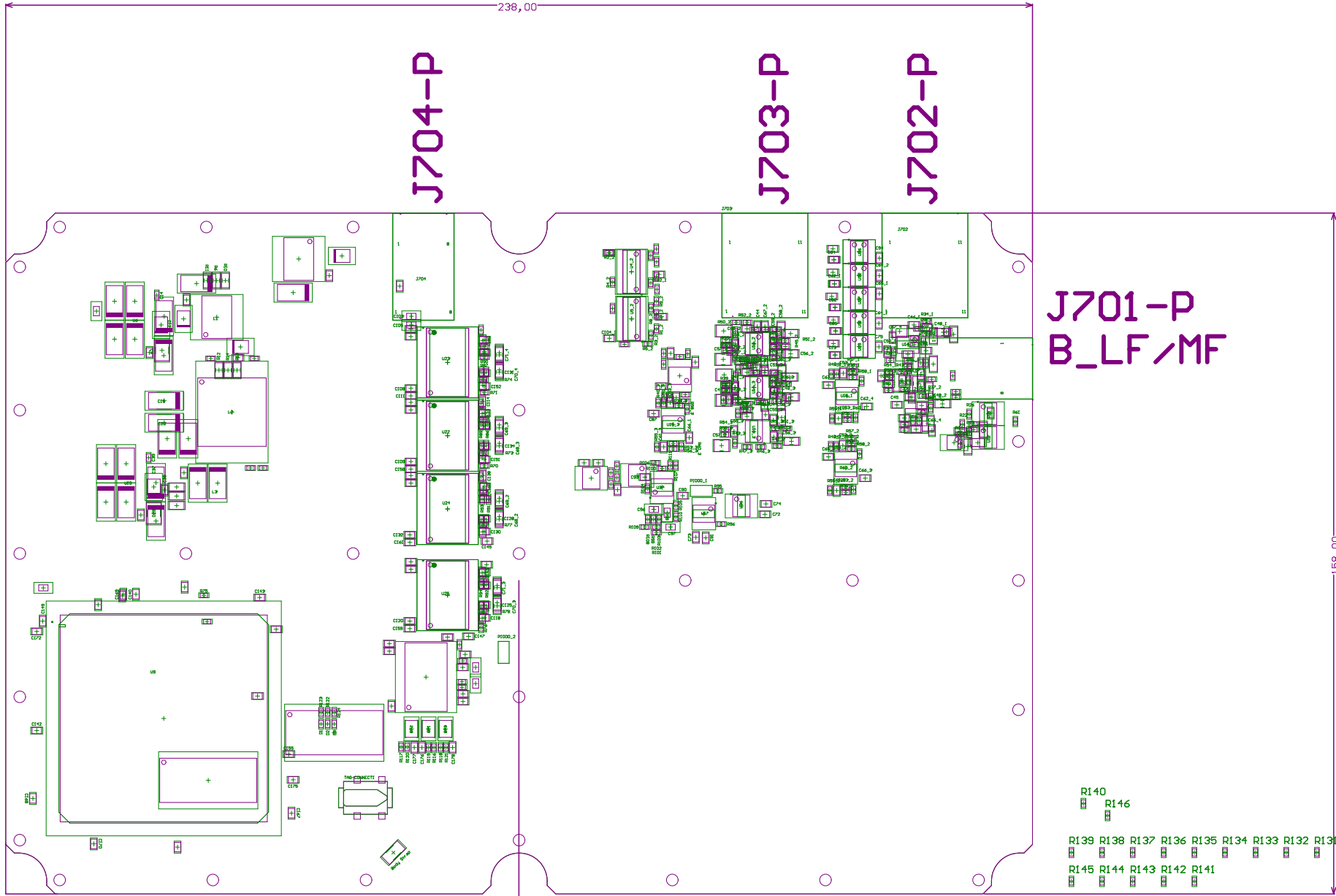
J704-P

J703-P

J702-P

J701-P
B_LF/MF

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R140
 R146

R139 R138 R137 R136 R135 R134 R133 R132 R131 R130 R129 R48 R44 R33 R29
 R145 R144 R143 R142 R141

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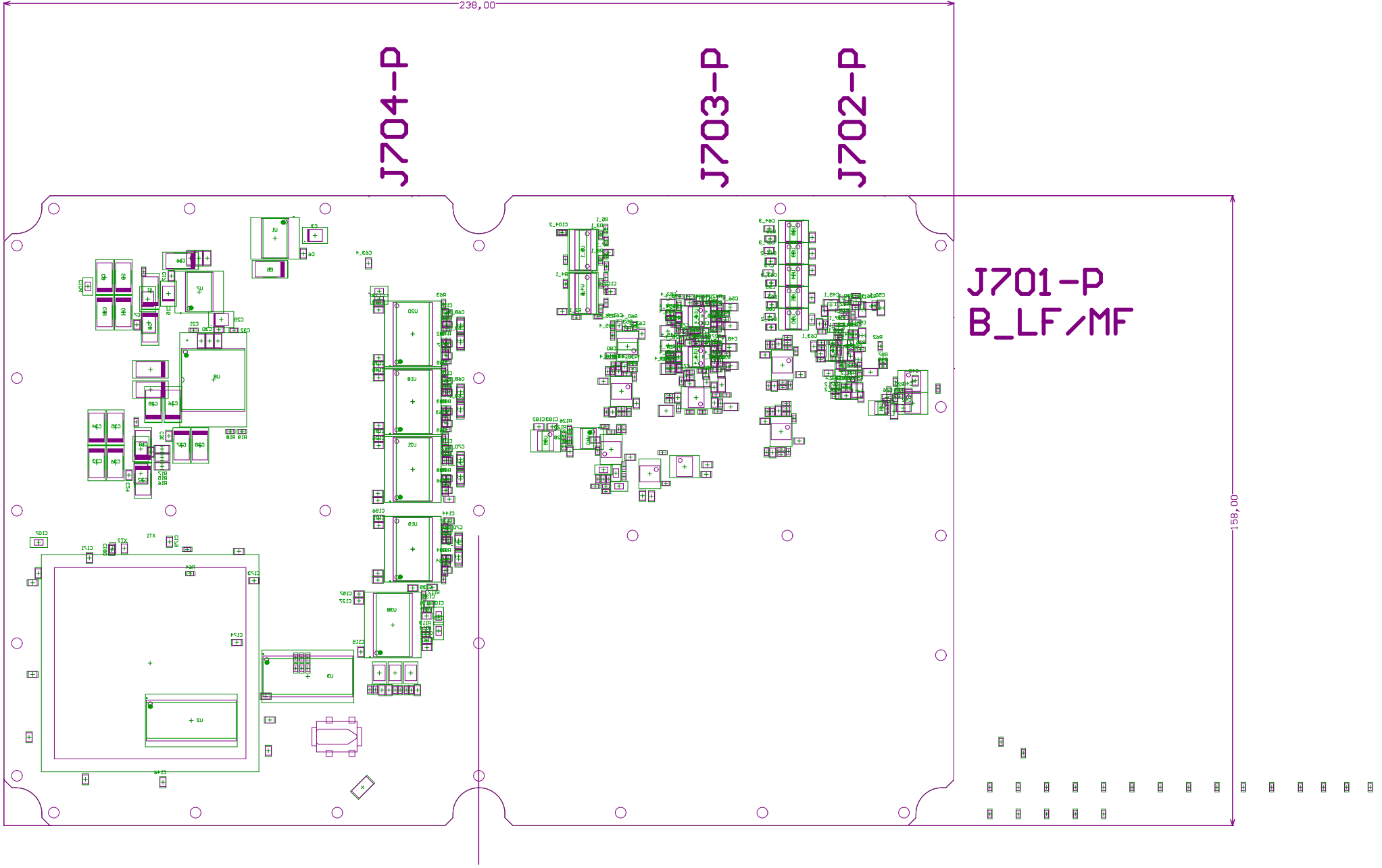
J704-P

J703-P

J702-P

J701-P
B_LF/MF

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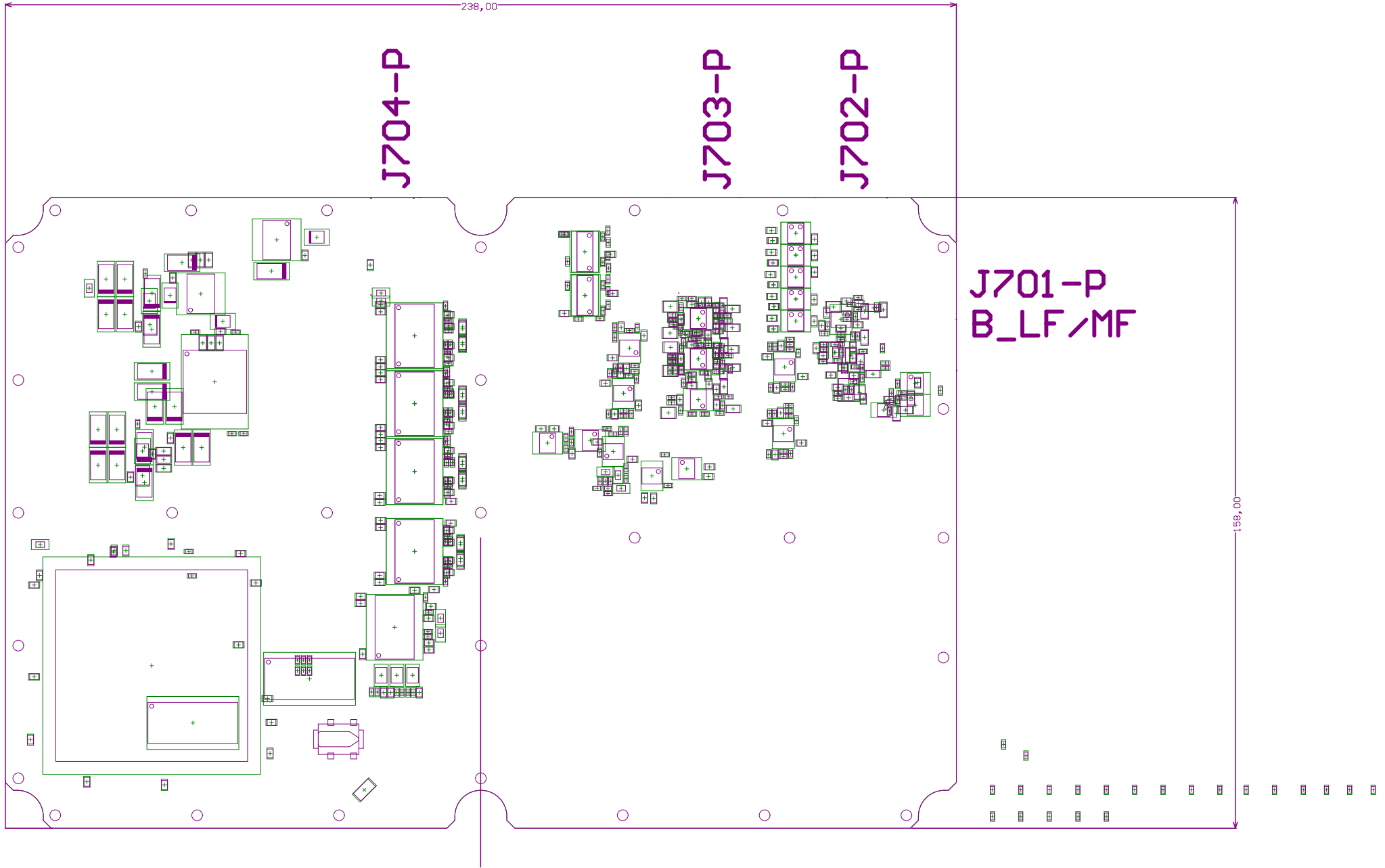
J704-P

J703-P

J702-P

J701-P
B_LF/MF

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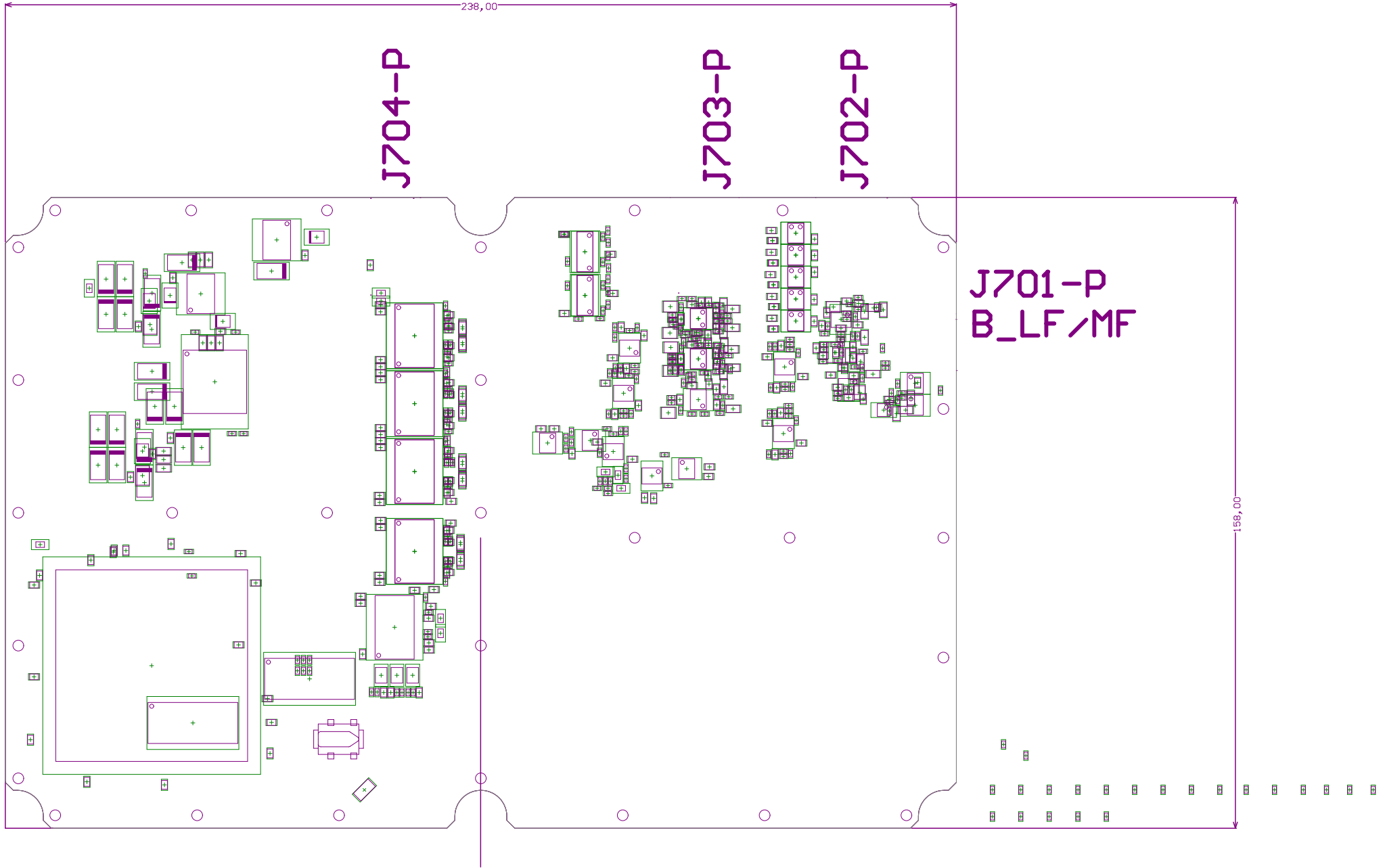
J704-P

J703-P

J702-P

J701-P
B_LF/MF

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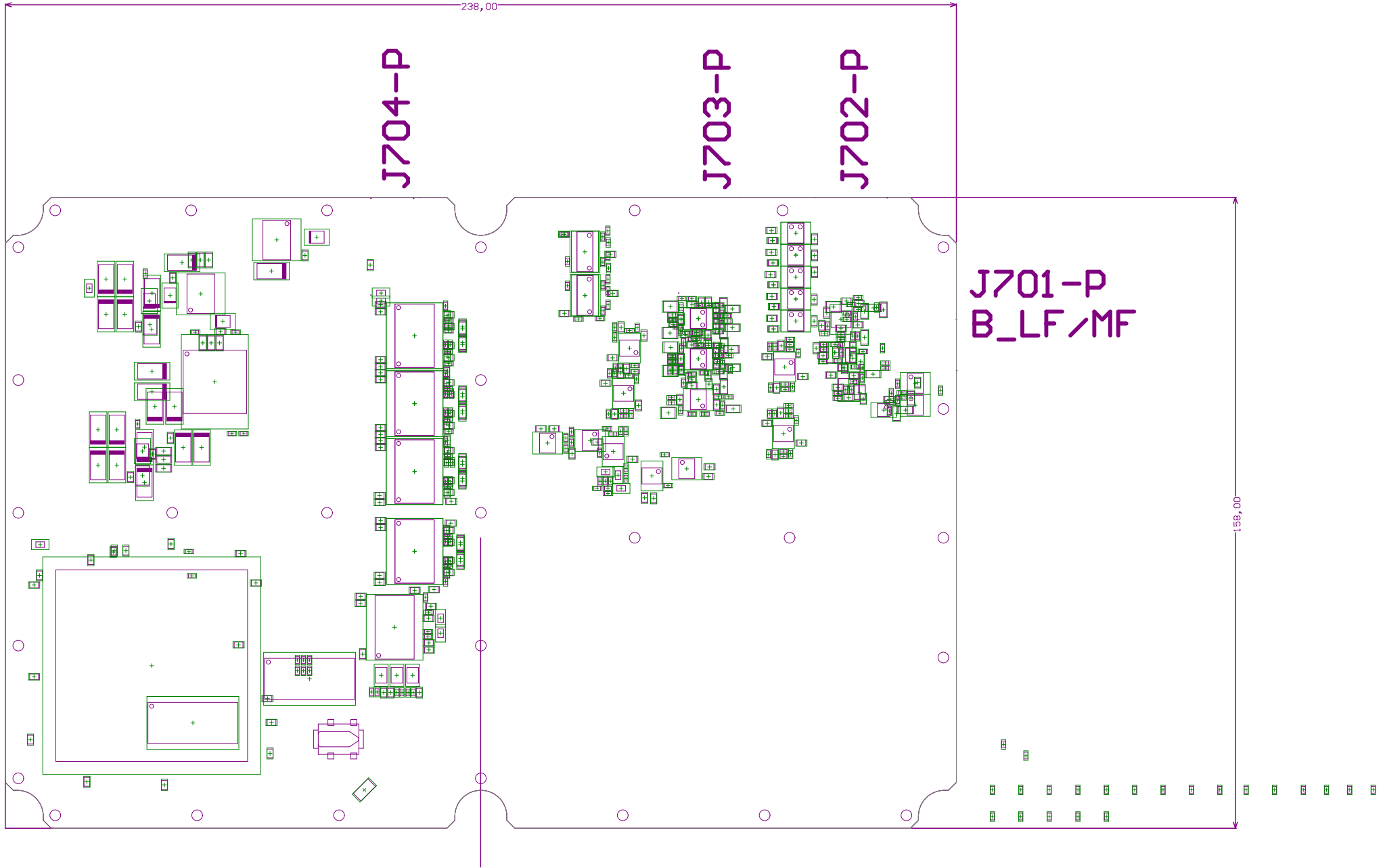
J704-P

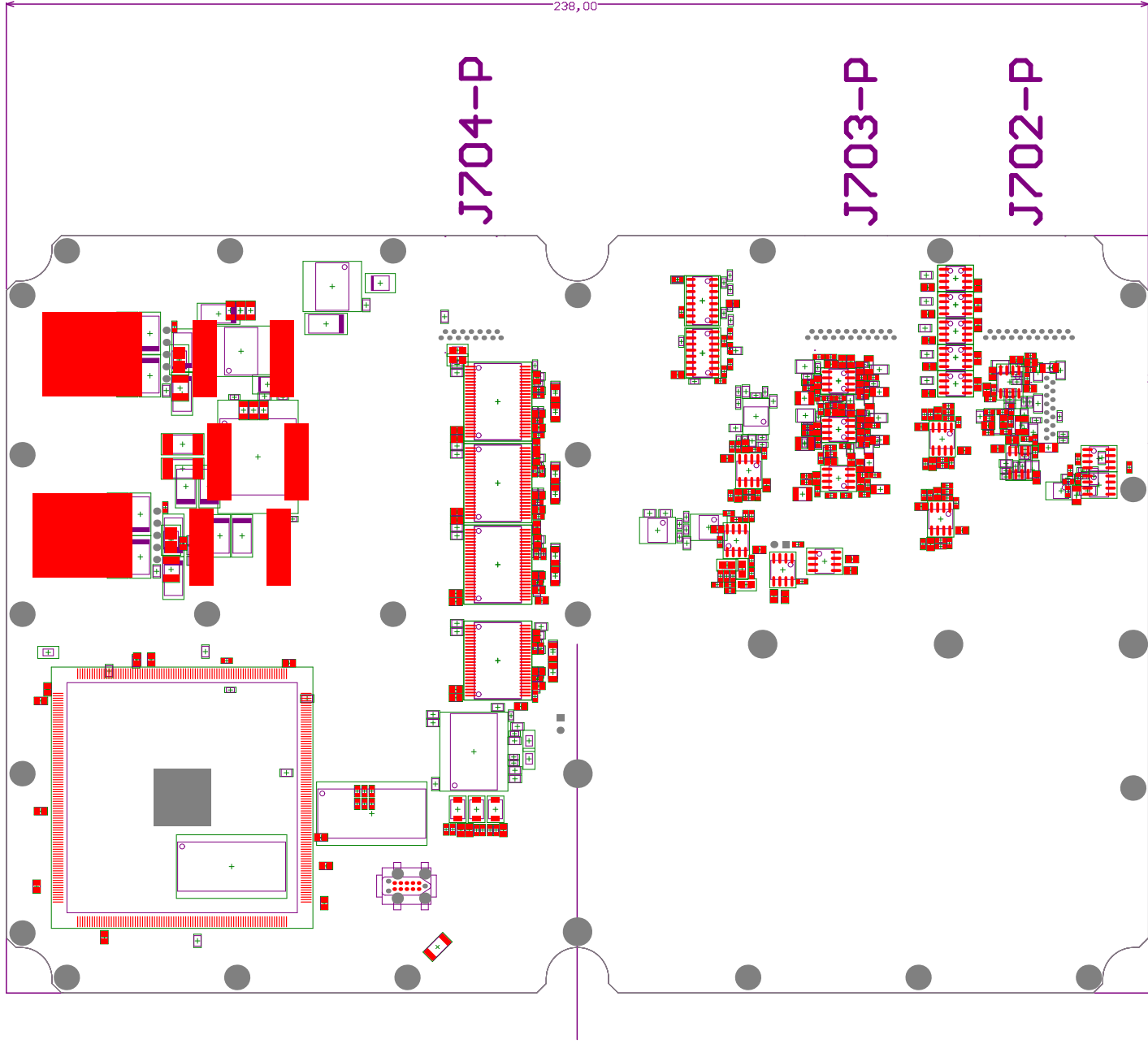
J703-P

J702-P

J701-P
B_LF/MF

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J704-P

J703-P

J702-P

J701-P
B_LF/MF

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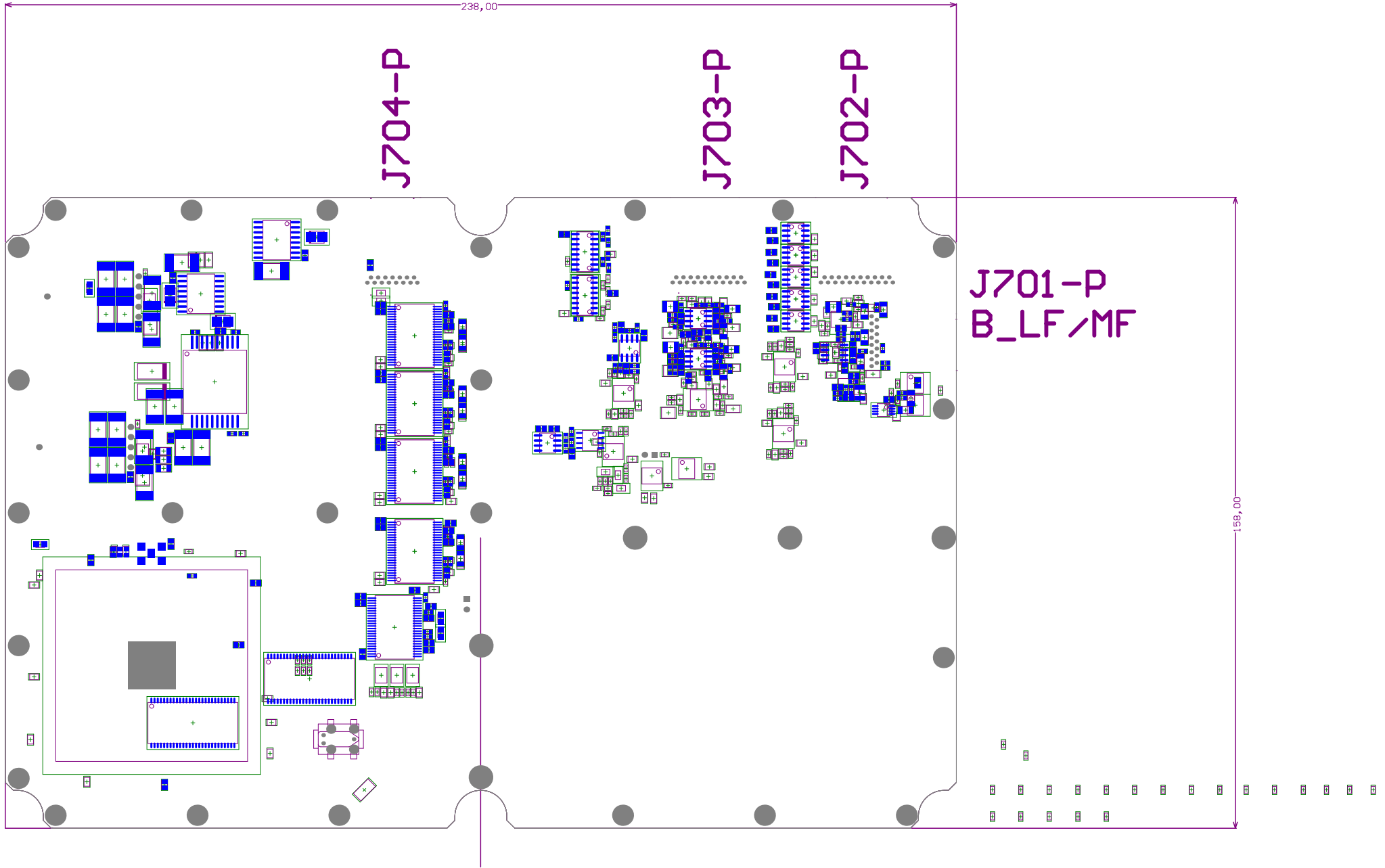
J704-P

J703-P

J702-P

J701-P
B_LF/MF

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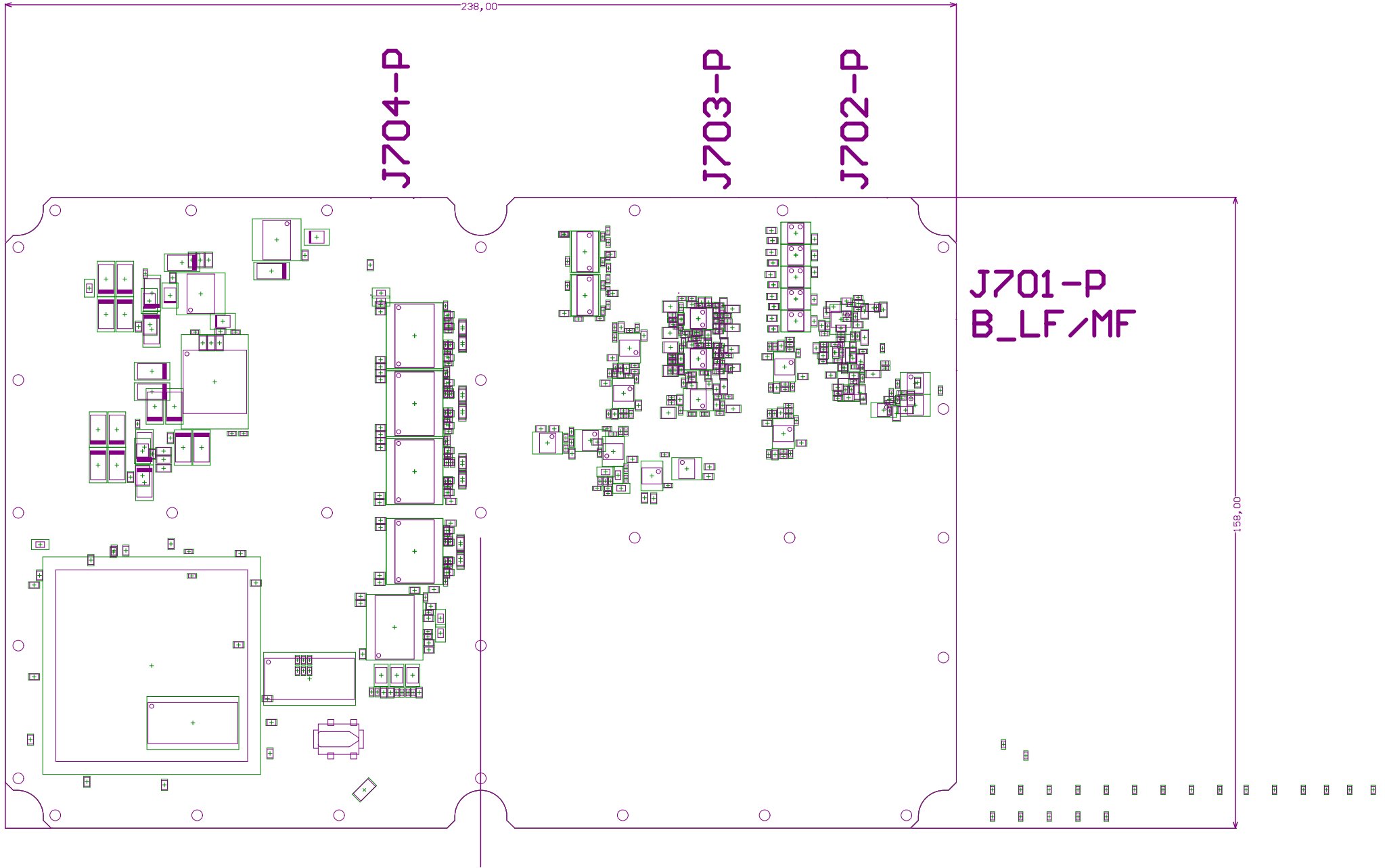
J704-P

J703-P

J702-P

J701-P
B_LF/MF

158,00



238,00

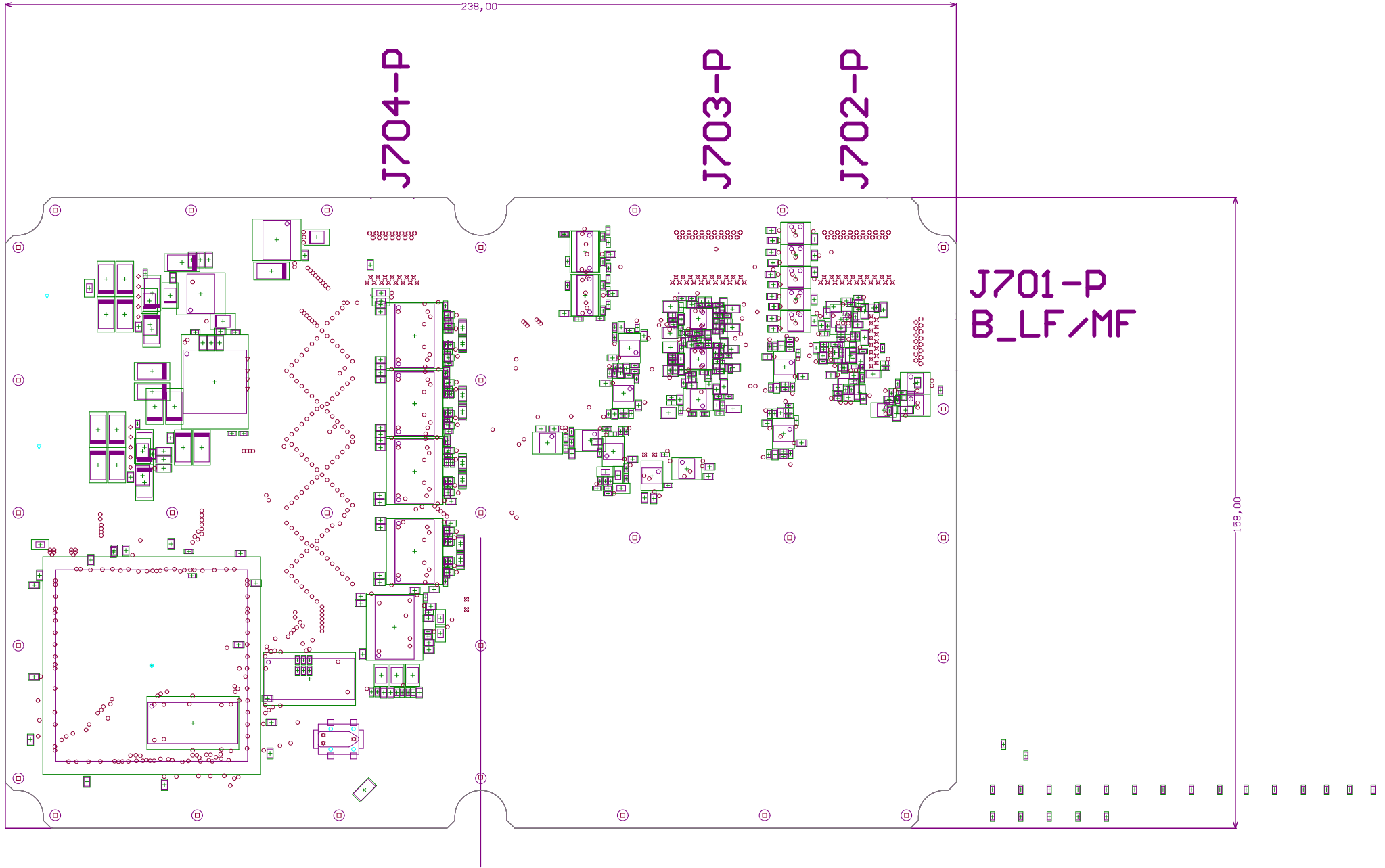
J704-P

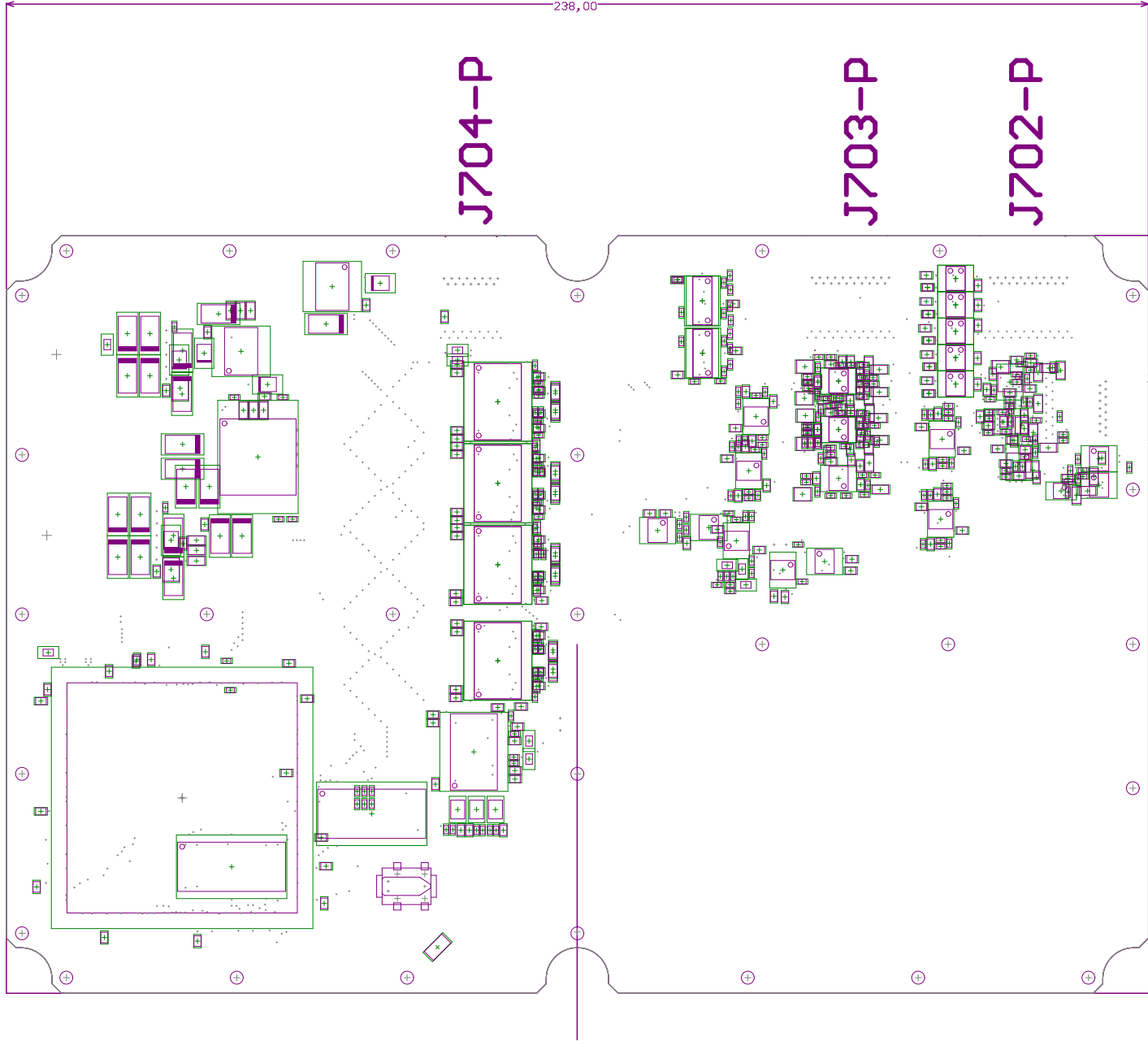
J703-P

J702-P

J701-P
B_LF/MF

158,00



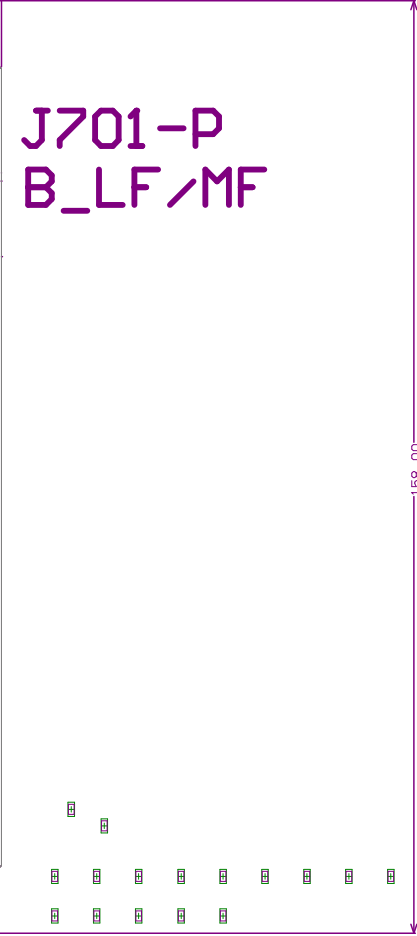


J704-P

J703-P

J702-P

238,00



J701-P
B_LF/MF

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