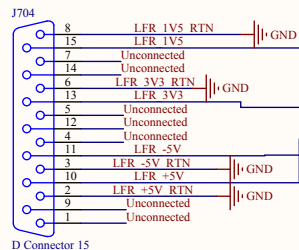
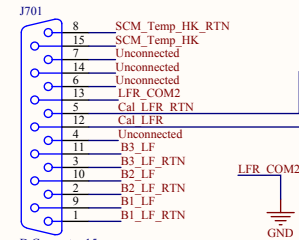


J704

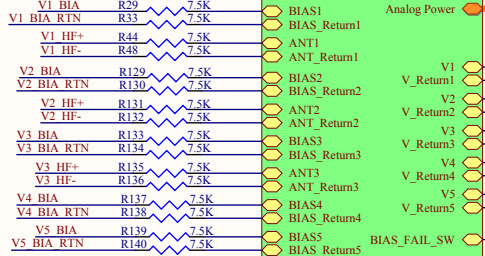


D Connector 15

J701

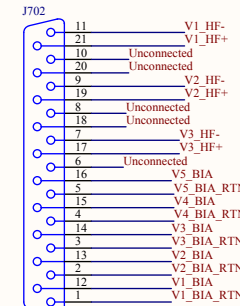


D Connector 15

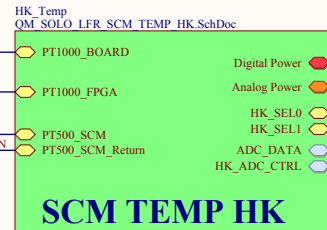
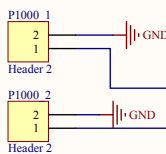


BIAS FAIL SW

J702

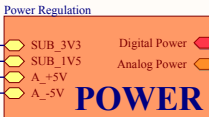


D Connector 21

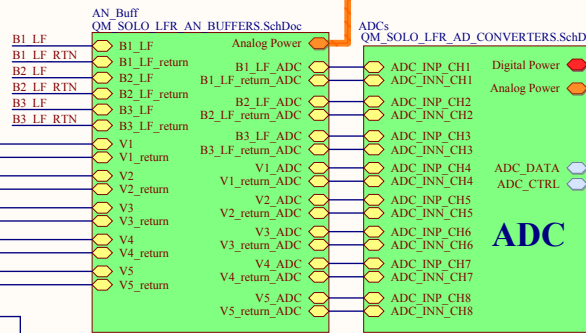


SCM TEMP HK

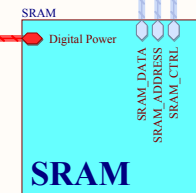
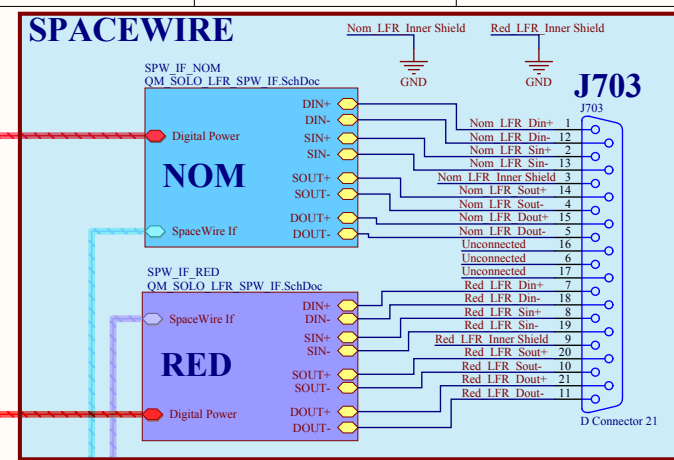
POWER



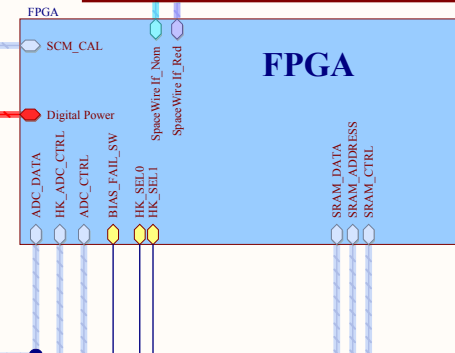
AN BUFFERS



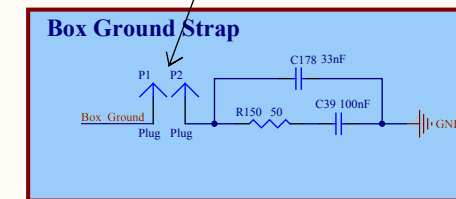
ADC



SRAM



FPGA



Box Ground Strap

Need discussion with Vincent

CHANGELOG

Title LFR_QM_TOP		Author: Alexis Jeandet		Laboratoire LPP	
Size: A3	Number: LFR-172200-FM	Revision: 01.04		Ecole Polytechnique	
Date: 30/06/2014	Time: 11:49:54	Sheet 1 of 12		Route de Saclay	
Contact: alexis.jeandet@lpp.polytechnique.fr				F-91128 Palaiseau	
File: F:\Missions\Satellites\SolarOrbiter\LFR\PCB\QM_SOLO_LFR_TOP_SchDoc				France	

CHANGELOG

09/04/2014

- Moved analog input buffers resistors before the swithes.
- C21 (100nF cap @ SUB1.5V input) footprint changed to 0805.
- Connected SENS input for RHFL4913 to Vout.
- 2.5V analogic connected to sub 3.3V.
- added R/C Slow start on 2.5V RHFL4913.
- 1.8V MSK5822 VBIAS input moved from 5V to sub 3.3V.

14/04/2014

- Connected SCM cal and SPW shield to GND.
- Unconnected Pin are connected to Unconnected Net which is tied to GND.

15/04/2014

- Updated ground strap, it's now removable and the circuit is a R C//R.

22/04/2014

- Connected 3.3V regulator VBIAS input to sub 3.3V.
- Connected MSKs Latch input to GND.
- Connected RHFL4913 INH inputs to GND.
- Replaced DG419 with 54HC4053 for bais/ant mux.

24/04/2014

- Replaced EM SRAM with FM SRAM UT8ER1M32.

25/04/2014

- Replaced DG419 with 54HC4053 for HK mux.
- Replaced DG419 with 54HC4053 for SCM CAL mux.
- Replaced DAC reference with qualified one.

30/04/2014

- Replaced EM Oscillators with FM.
- Replaced EM HK DAC with FM.

05/05/2014

- Added SPW enable signal.
- Replaced LT1009 by RH1009.
- Replaced MSK 3.3V regulator by RHFL4913.
- Added filtering structures on +/-5V.
- Added RC reset circuit for FPGA.
- Changed 400k resistors on ADC bias to 2x200k.

06/05/2014

- Changed power input inductors from 100μH to 10μH.

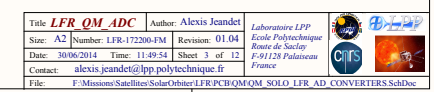
16/05/2014

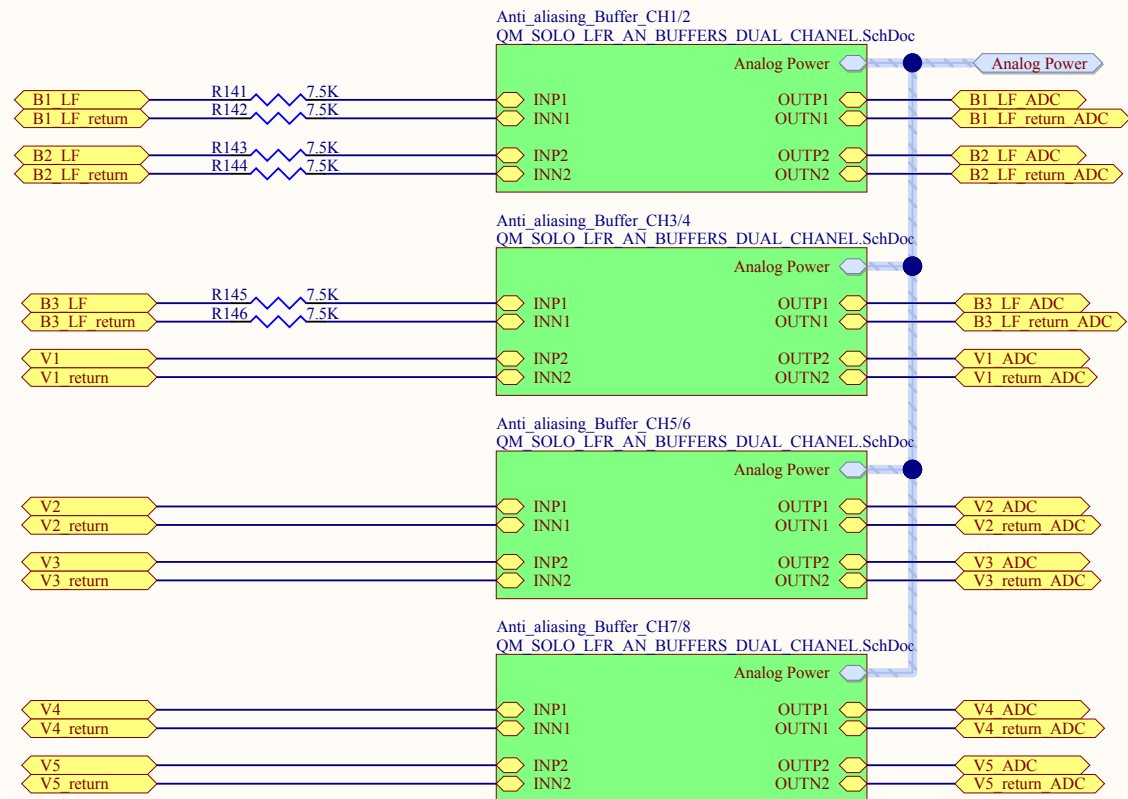
- Updated footprints from Vincent observations.

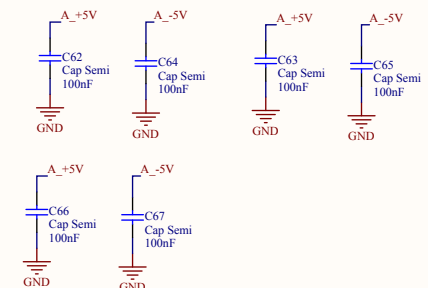
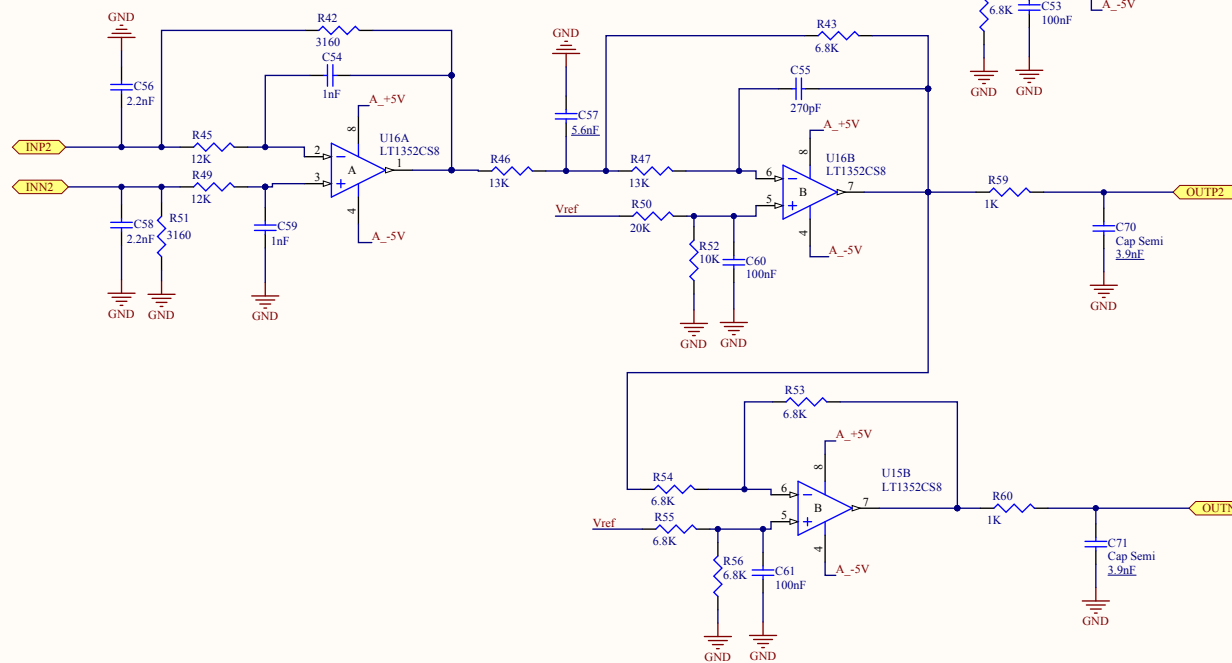
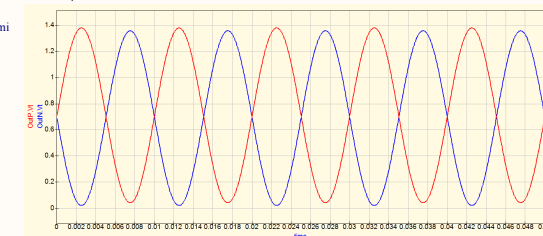
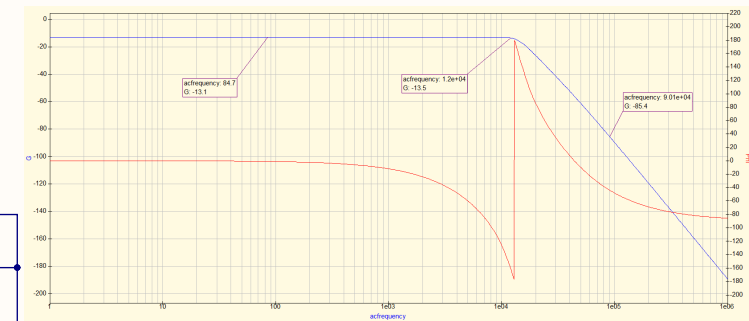
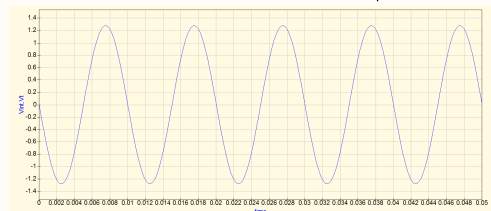
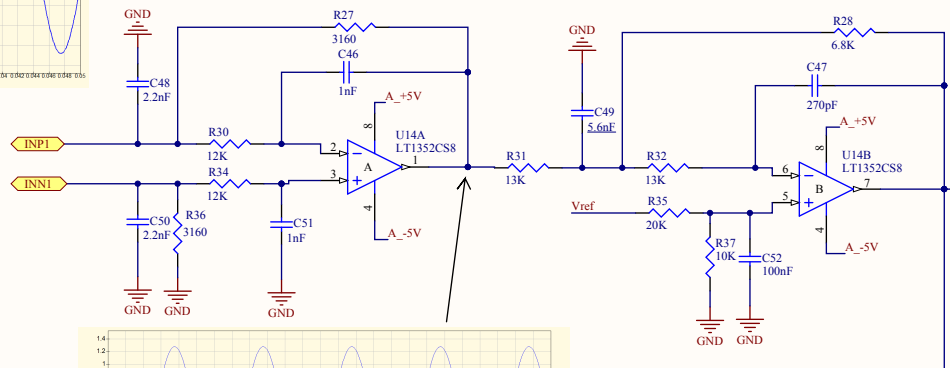
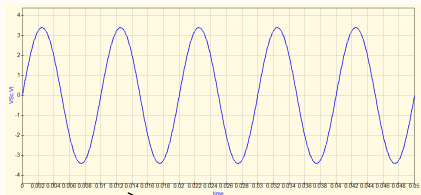
30/06/2014

- added reset connection on FPGA(mistake on 05/05/2014).
- Grounding strap update.

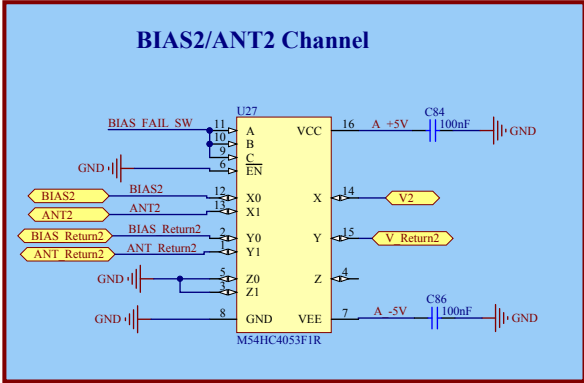
Title CHANGELOG		Author: Alexis Jeandet		Laboratoire LPP Ecole Polytechnique Route de Saclay F-91128 Palaiseau France 
Size: A4	Number: LFR-172200-FM	Revision: 01.04		
Date: 30/06/2014	Time: 11:49:54	Sheet 2 of 12		
Contact: alexis.jeandet@lpp.polytechnique.fr				
File: F:\Missions\Satellites\SolarOrbiter\LFR\PCB\QM\QM_CHANGELOG.SchDoc				







BIAS1/ANT1 Channel



BIAS3/ANT3 Channel

The diagram illustrates the BIAS3/ANT3 Channel for the MS4HC4053F1R component. The component is shown in a yellow box with pins 1 through 16. The BIAS3 input is connected to pin 12, and the ANT3 input is connected to pin 13. The BIAS3 Return3 output is connected to pin 2, and the ANT3 Return3 output is connected to pin 3. The component is powered by VCC (pin 16) and VEE (pin 7). The BIAS3 input is connected to pin 12, and the ANT3 input is connected to pin 13. The BIAS3 Return3 output is connected to pin 2, and the ANT3 Return3 output is connected to pin 3. The component is also connected to ground (GND) at pins 1, 4, 5, 6, 8, 9, 10, 11, 14, 15, and 16. The component is labeled MS4HC4053F1R.

BIAS4 Channel

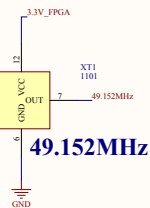
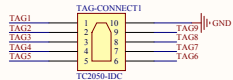
M54HC4053F1R

BIAS5 Channel

M54HC4053F1R



TAG-Probe



49.152MHz
QM&FM @50MHz
BBM,DM&EM @100MHz

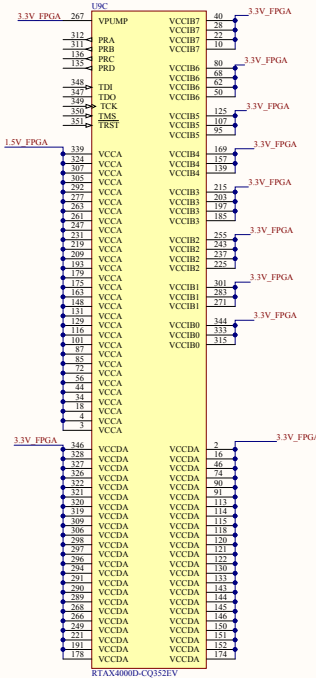
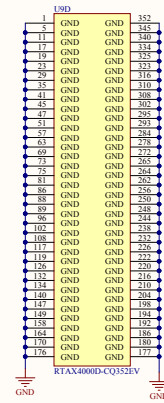
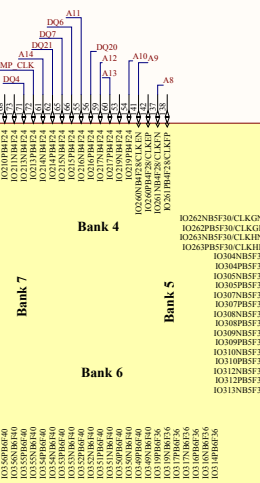
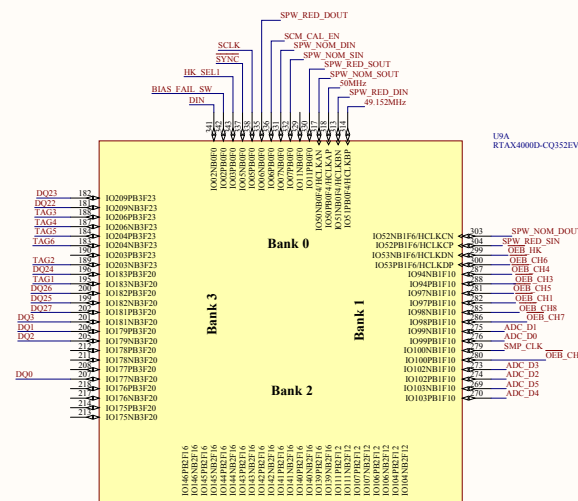
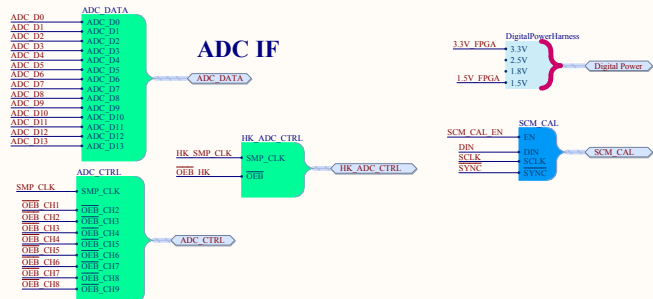
SPW Nominal Link



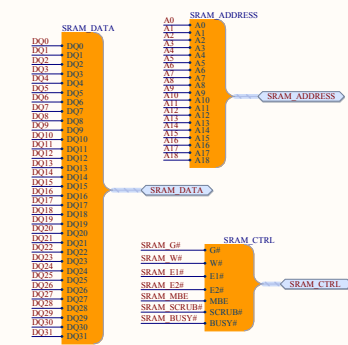
SPW Redundant Link



ADC IF



SRAM IF



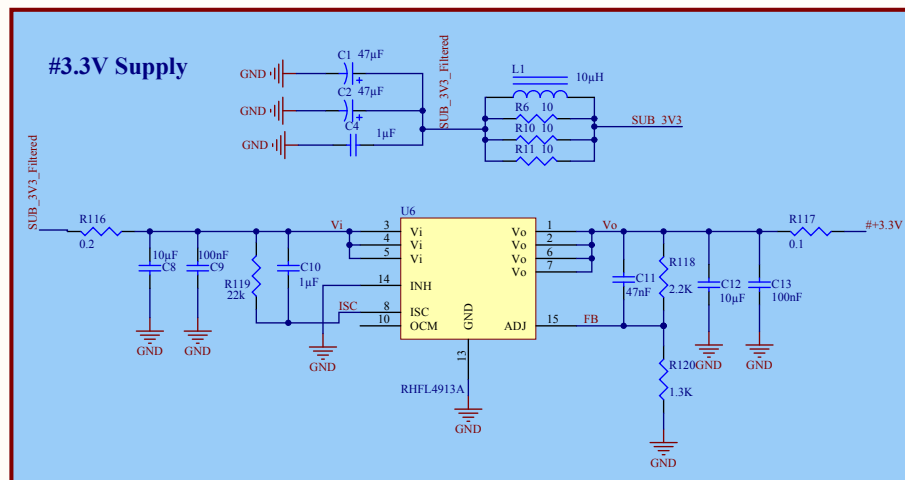
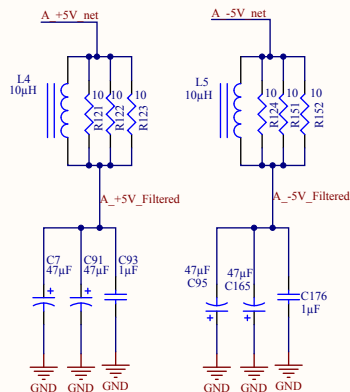
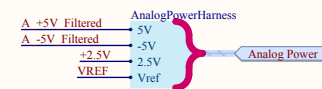
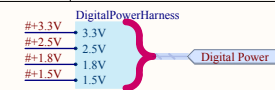
Characterization

Power-Up Characterization

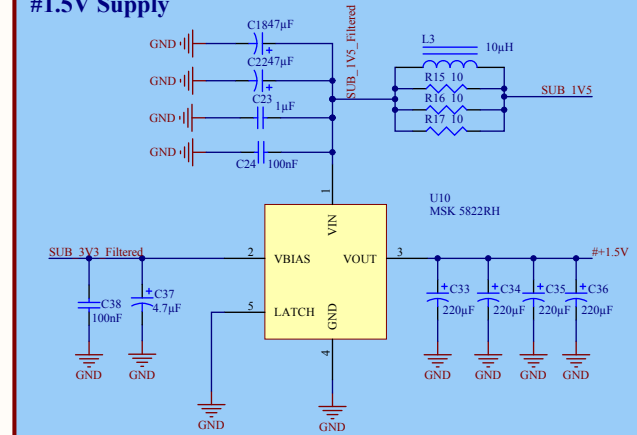
Power supplies for the RTAX-S/SL devices can power up in any sequence. Figure 1 and Figure 2 show the power-up characteristics for the different sequencing between VCCA (1.5 V) and VCCDA/VCCIBx (3.3 V). No significant transient current (>5 mA) is observed with either sequence.

Uses Rev H for MSK5822 and MSK5810 regulators documentation!

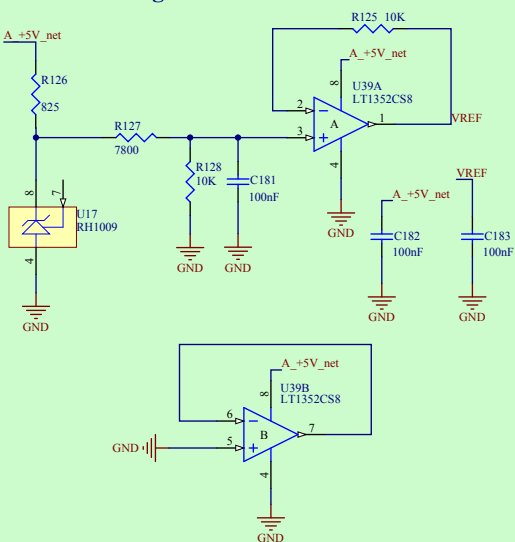
220uF => TAZ-H package
47uF => TAZ-H package
4.7uF => TAJ-B package



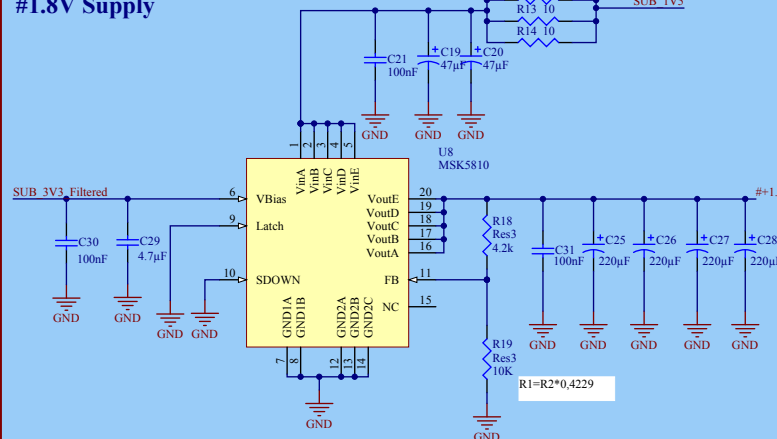
#1.5V Supply



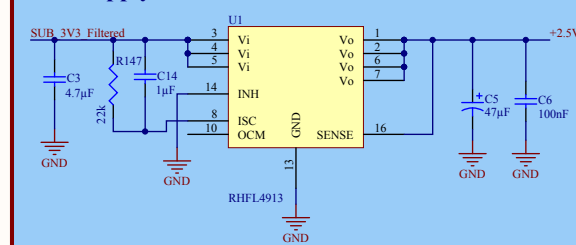
Reference Voltage 1.4V



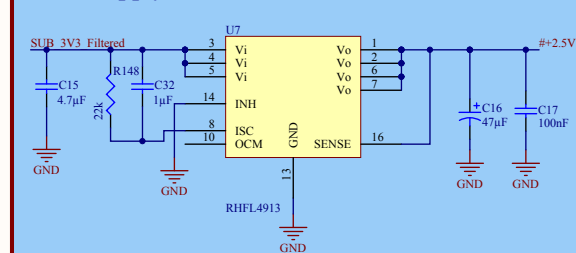
#1.8V Supply



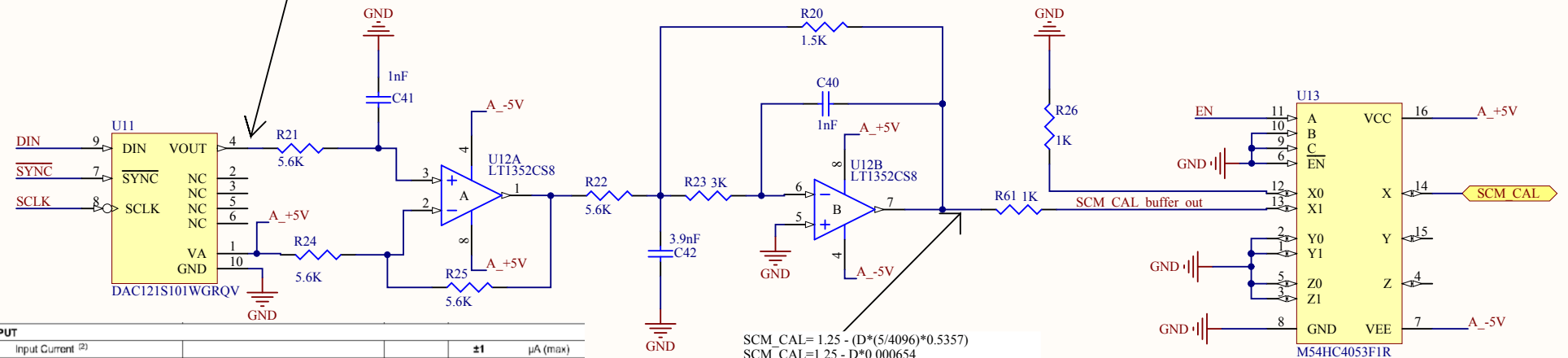
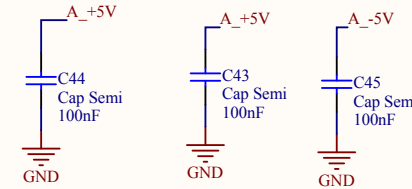
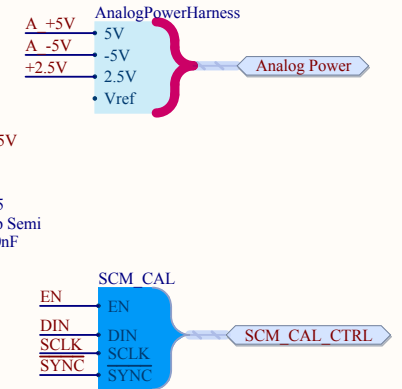
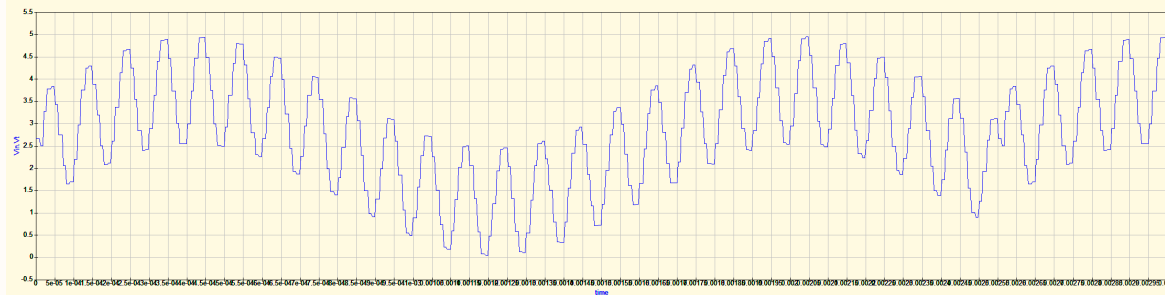
2.5V Supply



#2.5V Supply



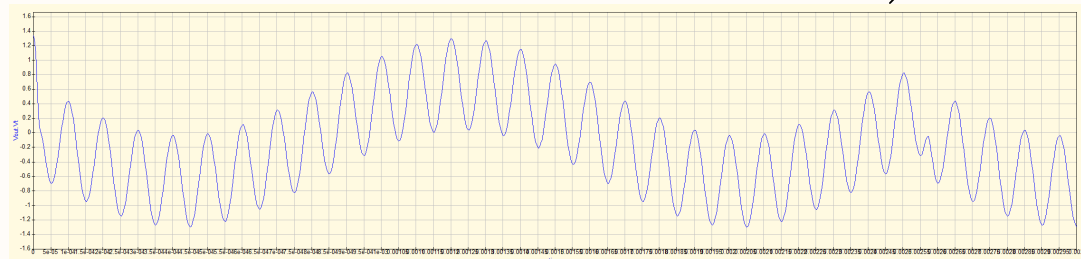
REQ-RPW-LFR-4706 LFR shall deliver a calibration signal to the SCM. This signal will be the sum of two sinus waves, at different frequencies $f_1 = 625$ Hz and $f_2 = 10$ kHz, with amplitudes of 500 mVpp, a sampling frequency of [TBD], a resolution of 8 bits and a duration of 4 s.
When not used, the calibration signal will be tied to ground (TBC) via an analog switch.



LOGIC INPUT			
I_{IH}	Input Current ⁽²⁾		± 1 μA (max)
V_{IL}	Input Low Voltage ⁽²⁾	$V_A = 5V$	0.8 V (max)
		$V_A = 3V$	0.5 V (max)
V_{HI}	Input High Voltage ⁽²⁾	$V_A = 5V$	2.4 V (min)
		$V_A = 3V$	2.1 V (min)
C_{IN}	Input Capacitance ⁽²⁾		3 pF (max)

$$SCM_CAL = 1.25 - (D * (5/4096) * 0.5357)$$

$$SCM_CAL = 1.25 - D * 0.000654$$



A

B

C

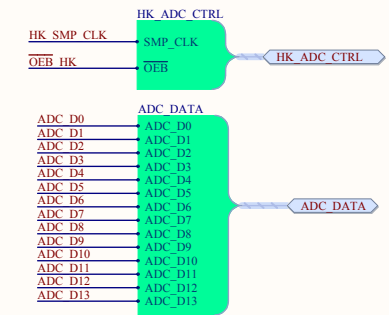
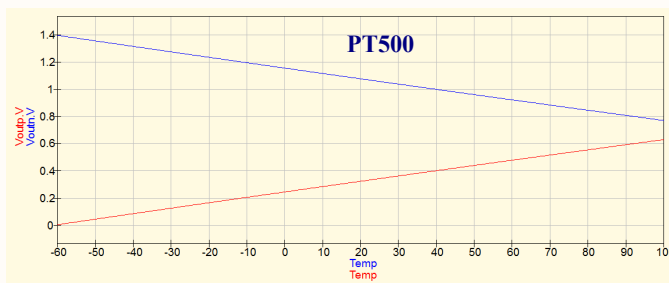
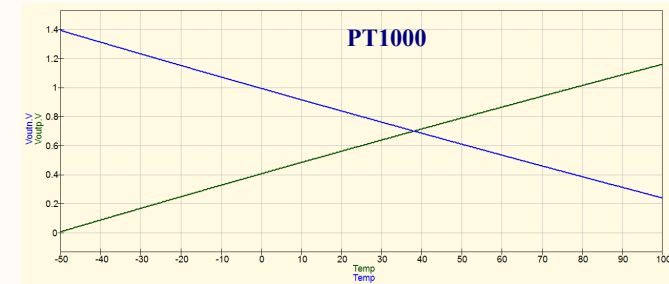
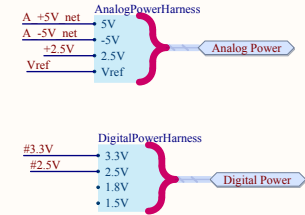
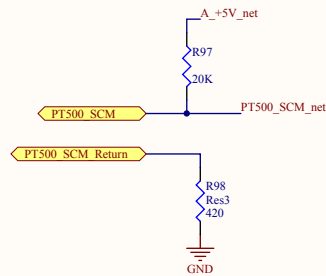
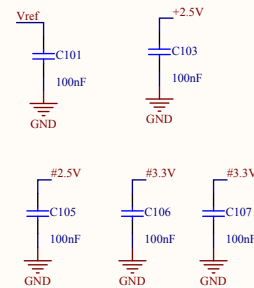
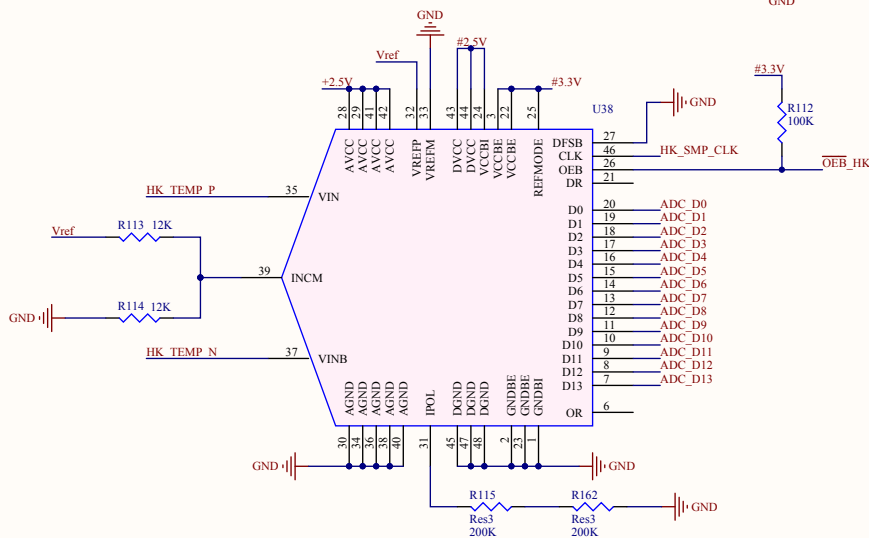
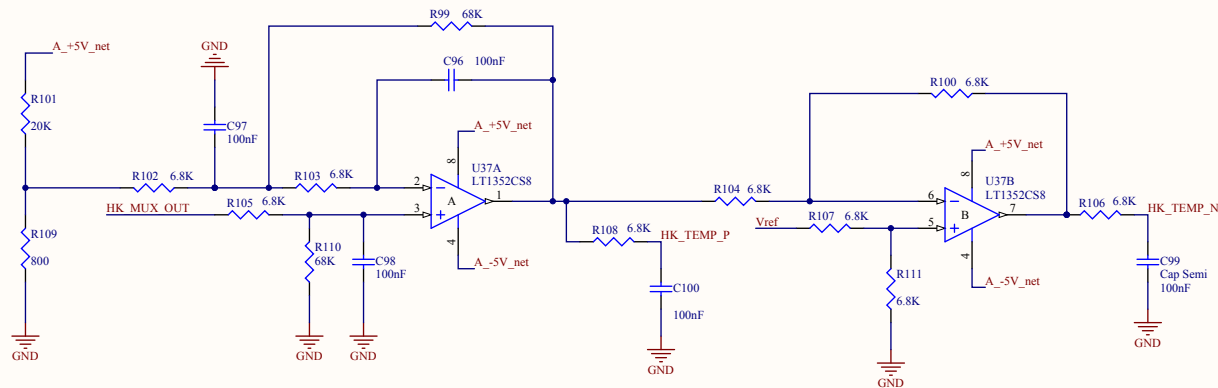
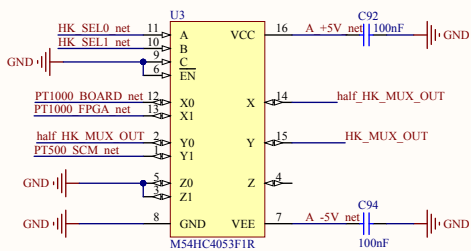
D

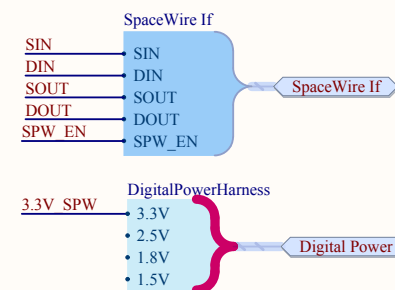
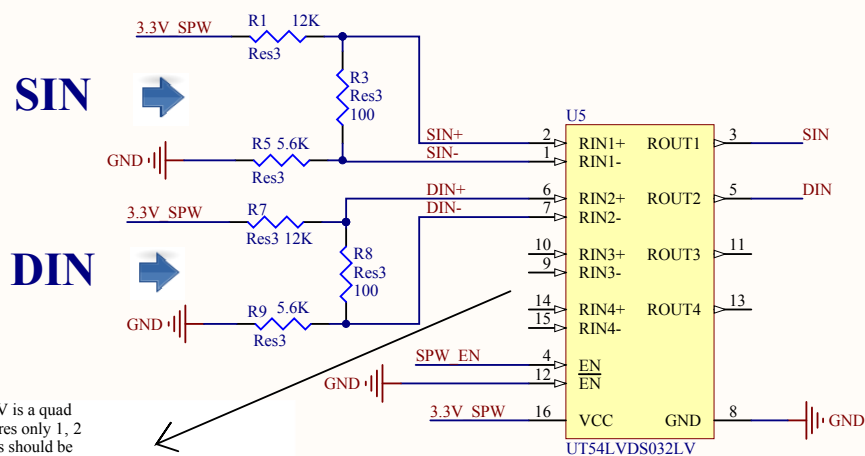
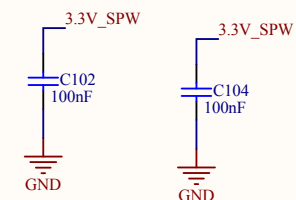
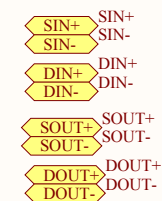
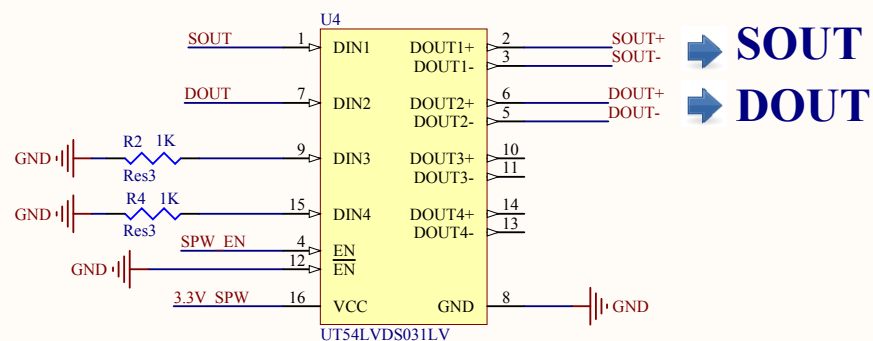
A

B

C

D





1. Open Input Pins. The UT54LVDS032LV is a quad receiver device, and if an application requires only 1, 2 or 3 receivers, the unused channel(s) inputs should be left OPEN. Do not tie unused receiver inputs to ground or any other voltages. The input is biased by internal high value pull up and pull down resistors to set the output to a HIGH state. This internal circuitry will guarantee a HIGH, stable output state for open inputs.

cf : <http://www.aeroflex.com/ams/pagesproduct/datasheets/LVDSReceiver3v.pdf>

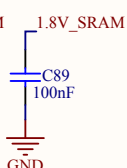
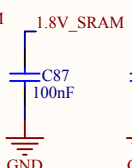
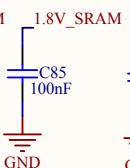
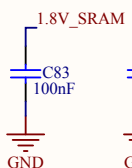
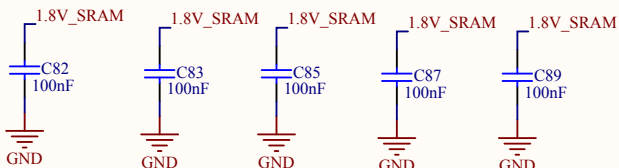
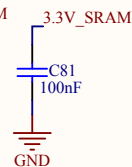
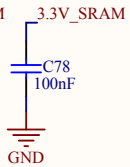
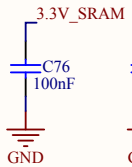
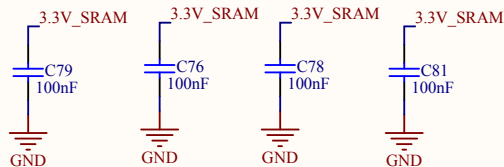
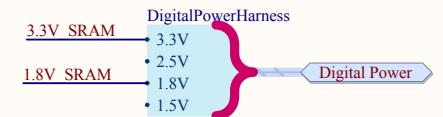
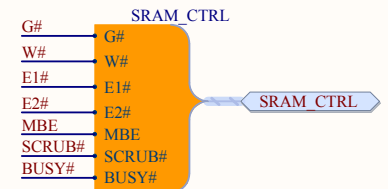
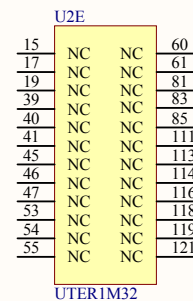
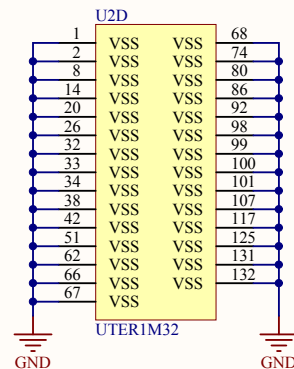
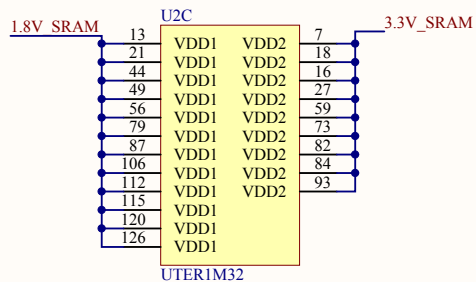
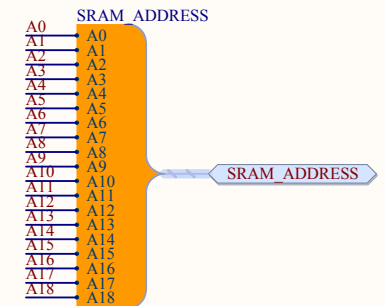
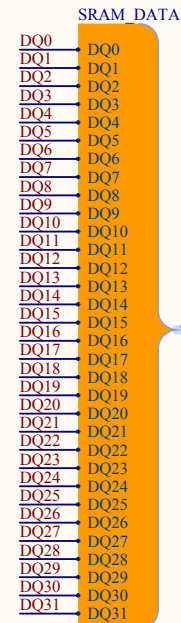
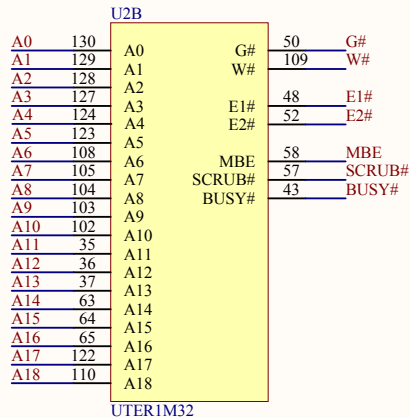
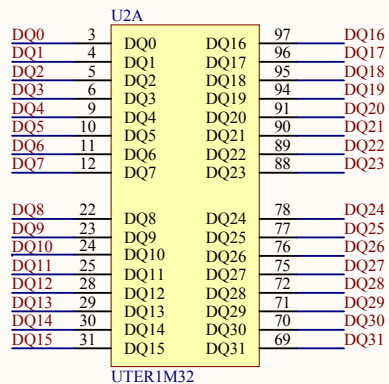
Title	LFR_QM_SPW	Author:	Alexis Jeandet	Laboratoire LPP	
Size:	A4	Number:	LFR-172200-FM	Revision:	01.04
Date:	30/06/2014	Time:	11:49:56	Sheet	11 of 12
Contact:	alexis.jeandet@lpp.polytechnique.fr			Ecole Polytechnique	
File:	F:\Missions\Satellites\SolarOrbiter\LFR\PCB\QM\QM_SOLO_LFR_SPW_IF.SchDoc			Route de Saclay	
				F-91128 Palaiseau	
				France	

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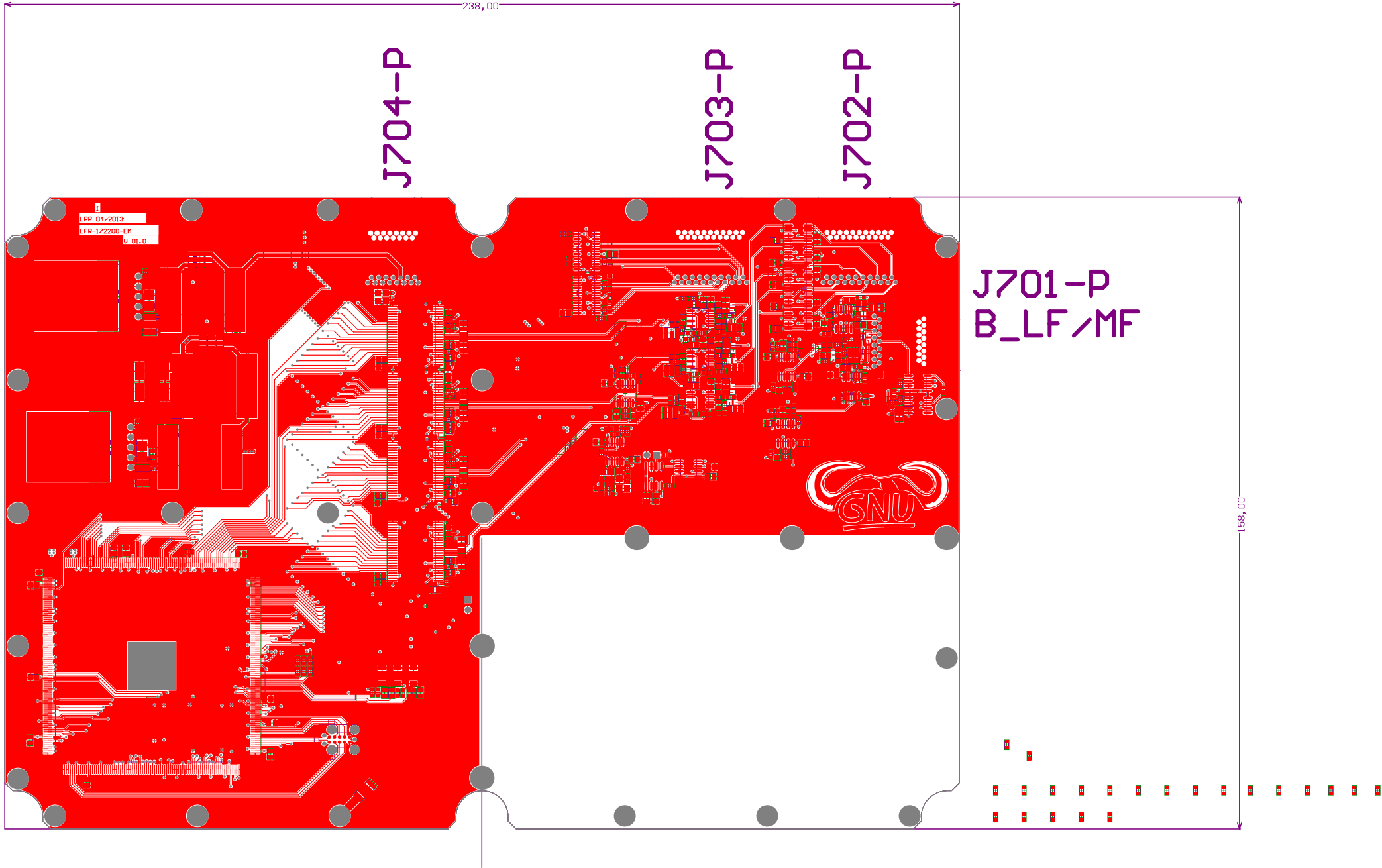
Title <i>LFR_QM_SRAM</i>		Author: Alexis Jeandet		Laboratoire LPP Ecole Polytechnique Route de Saclay F-91128 Palaiseau France	
Size: A4	Number: LFR-172200-FM	Revision: 01.04			
Date: 30/06/2014	Time: 11:49:56	Sheet 12 of 12			
Contact: alexis.jeandet@lpp.polytechnique.fr					
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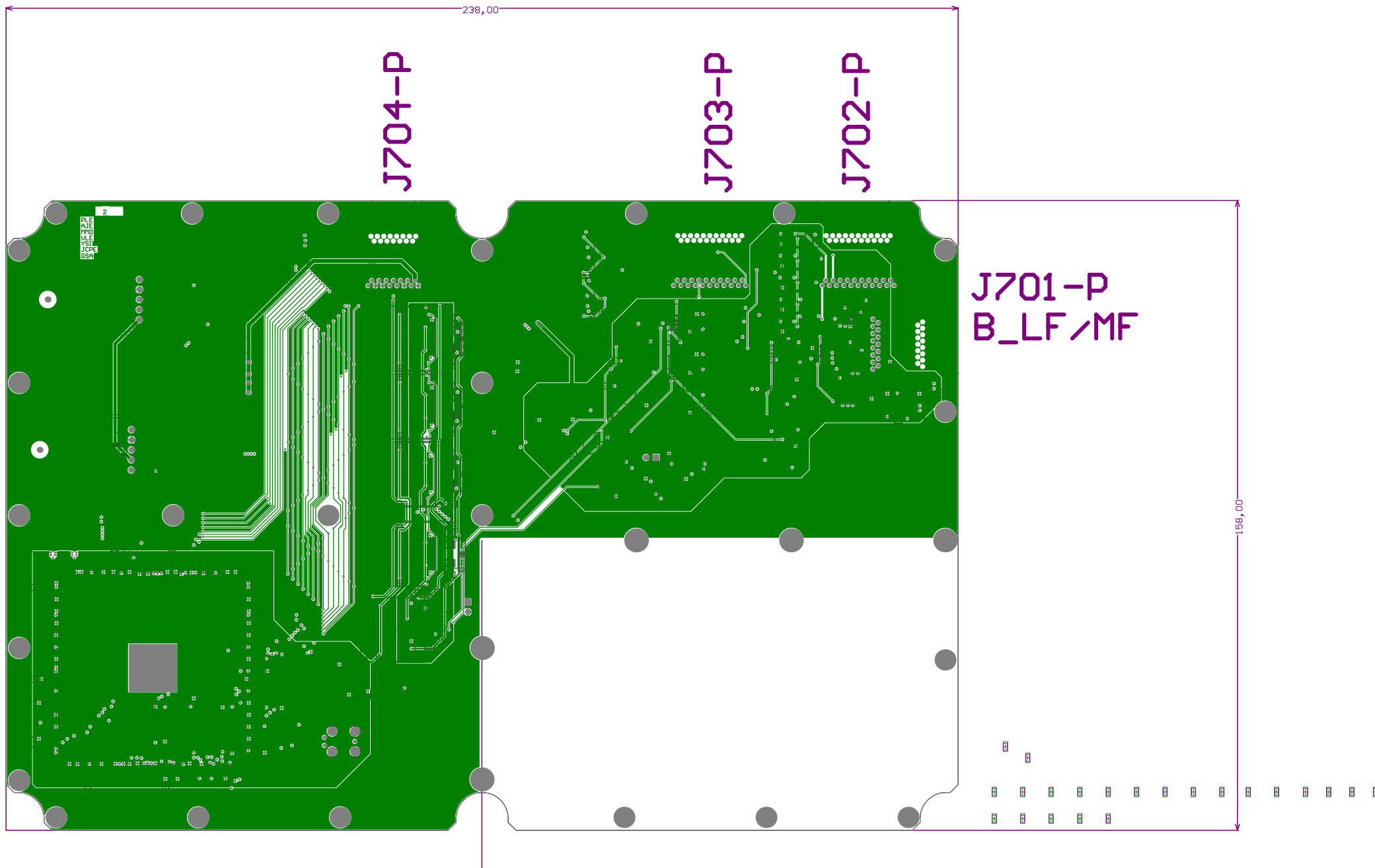
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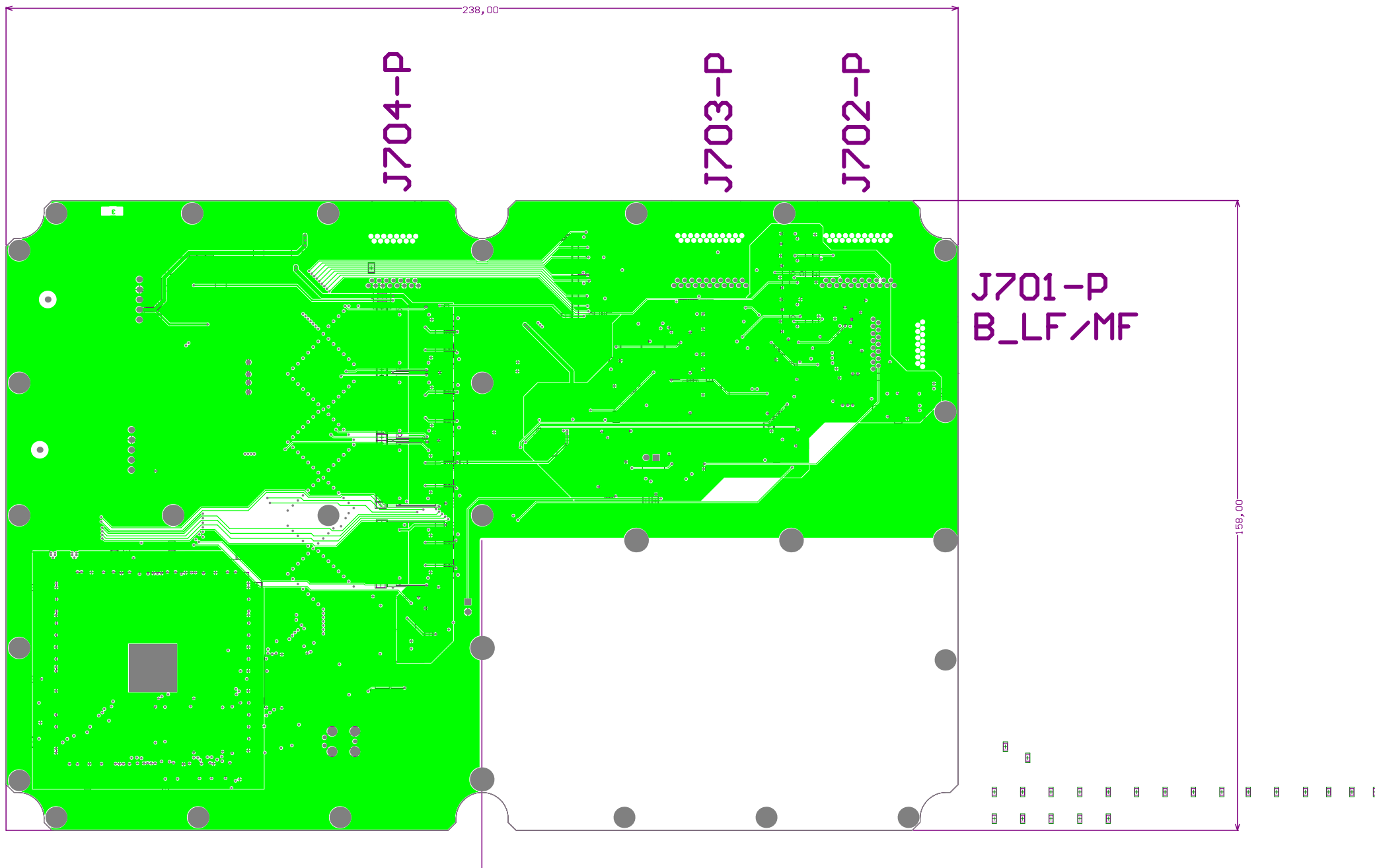
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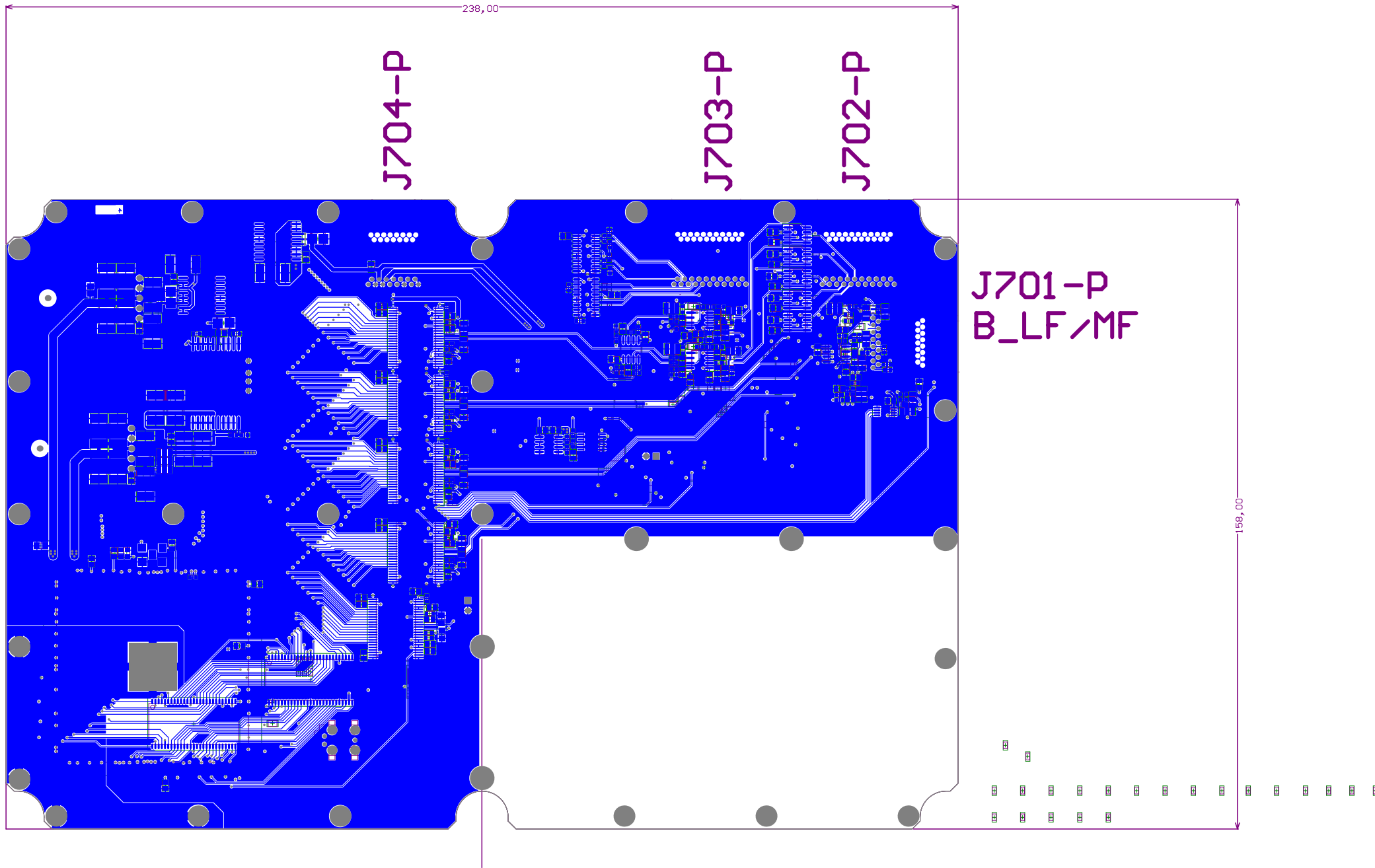
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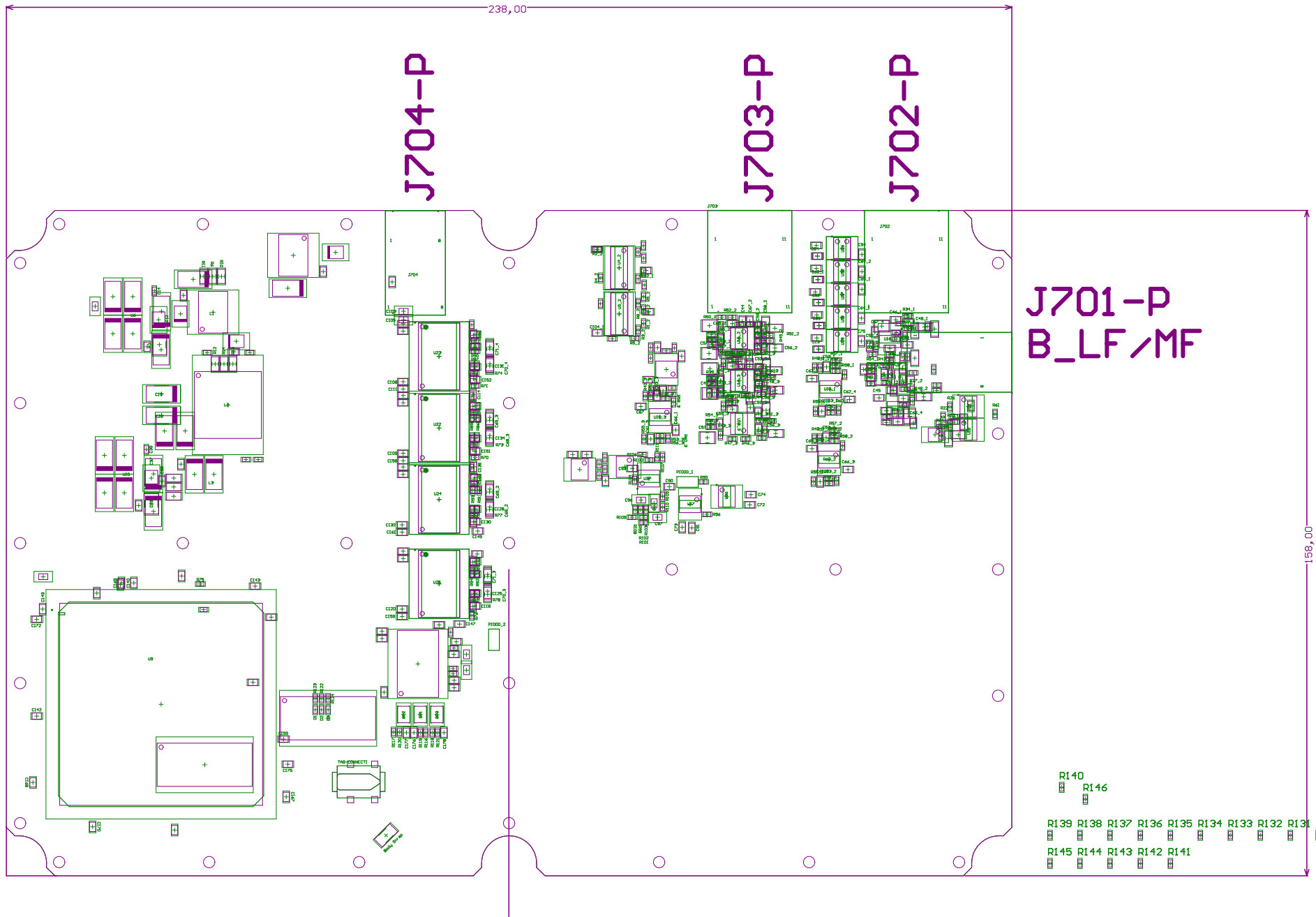
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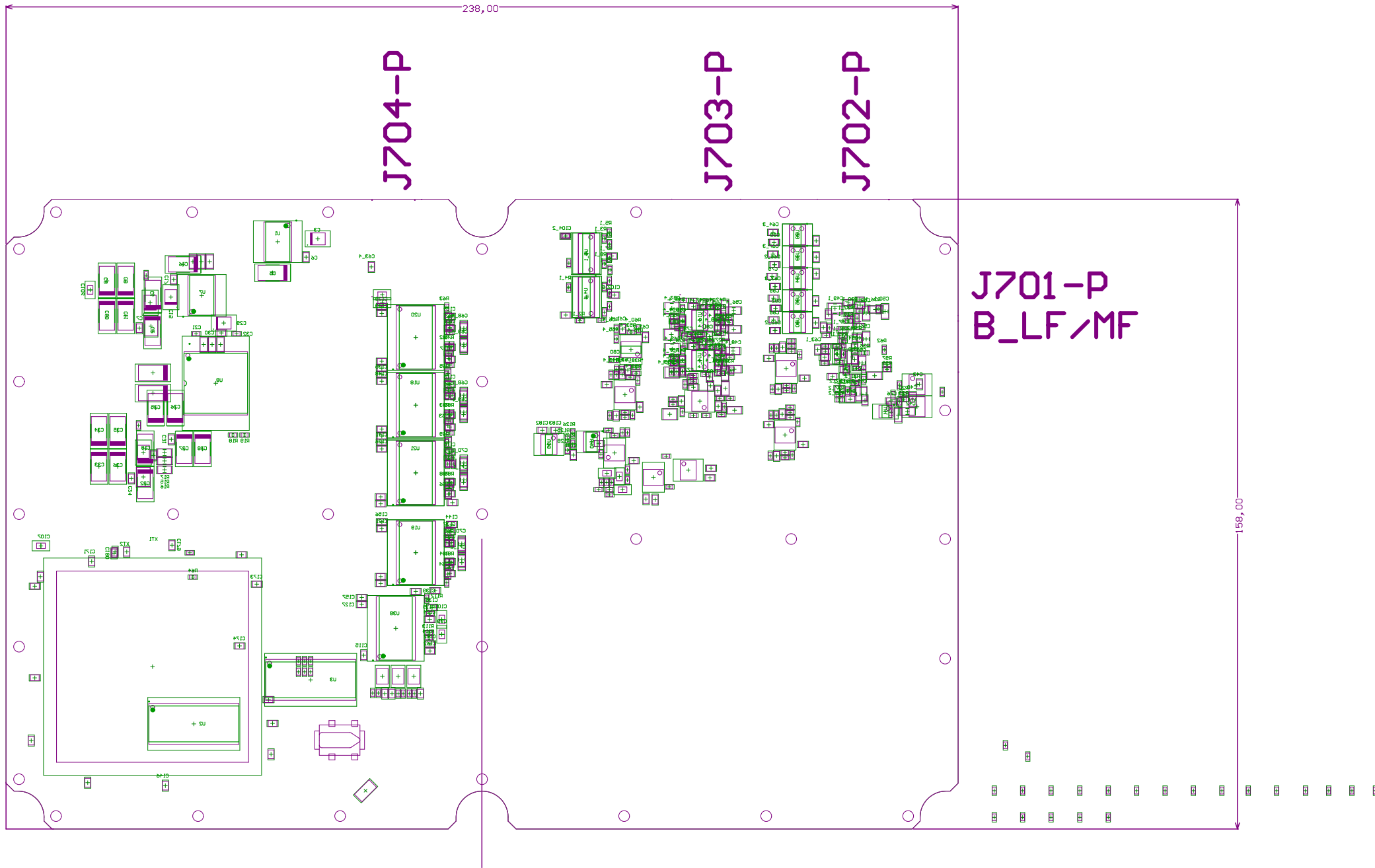
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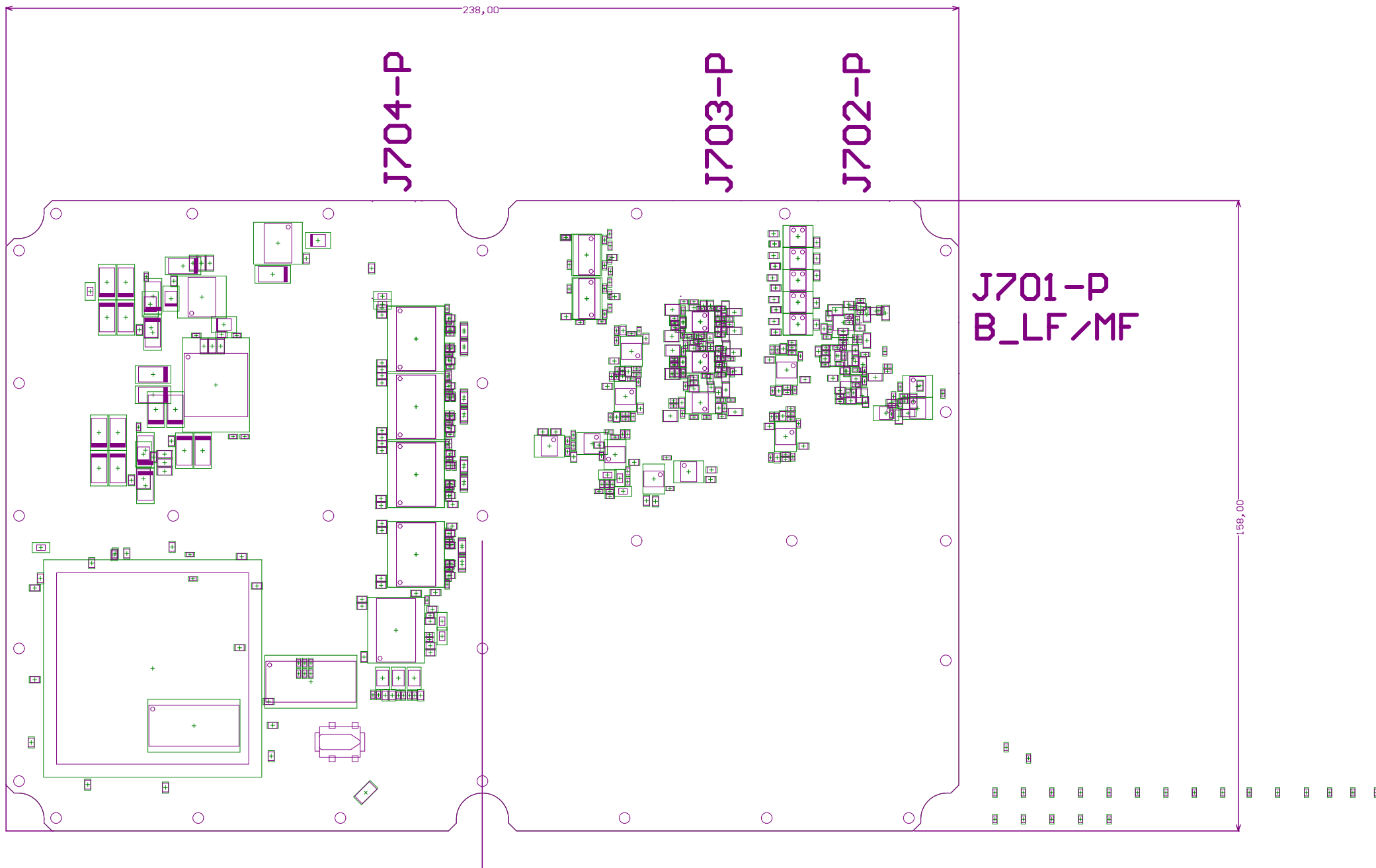
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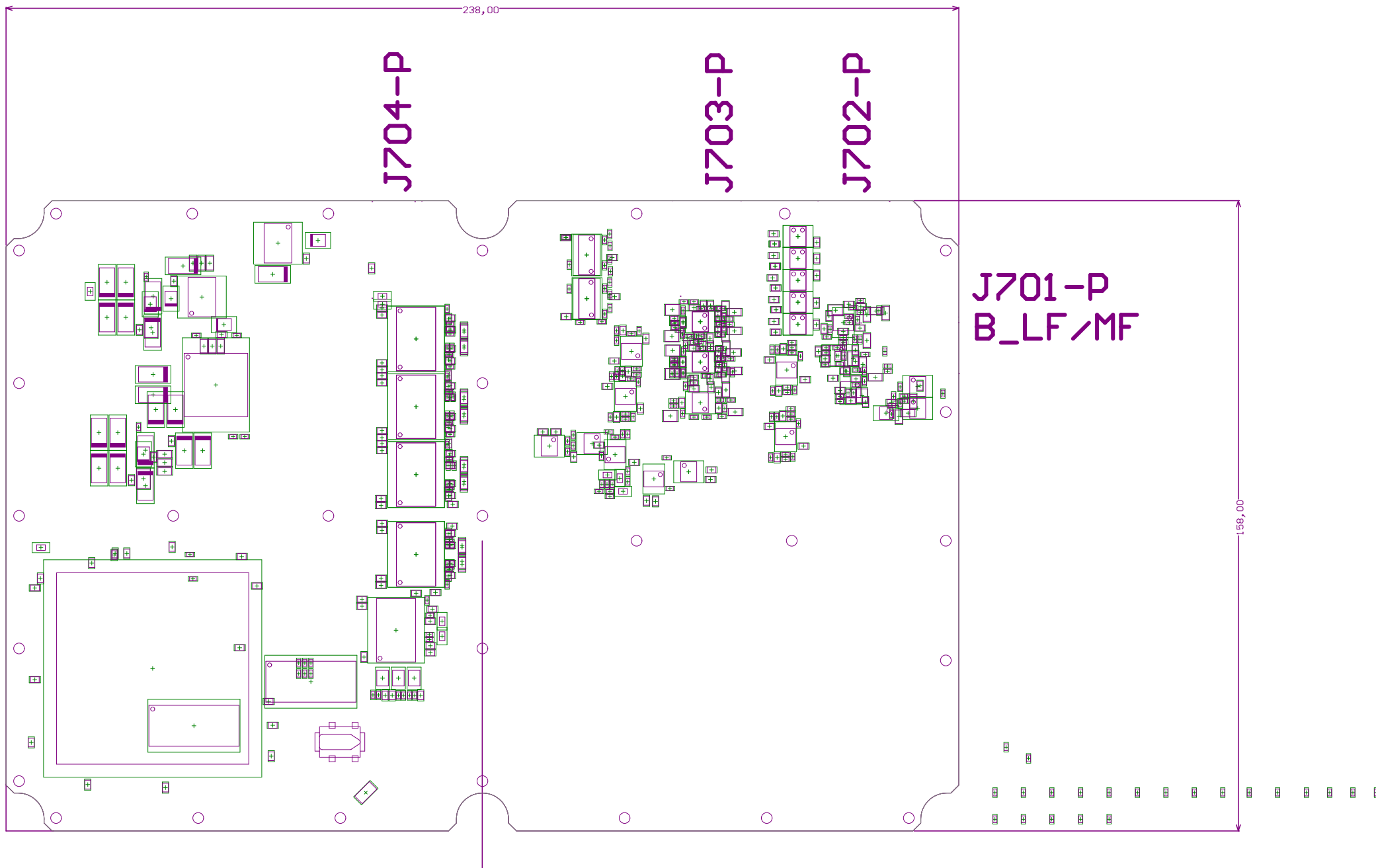
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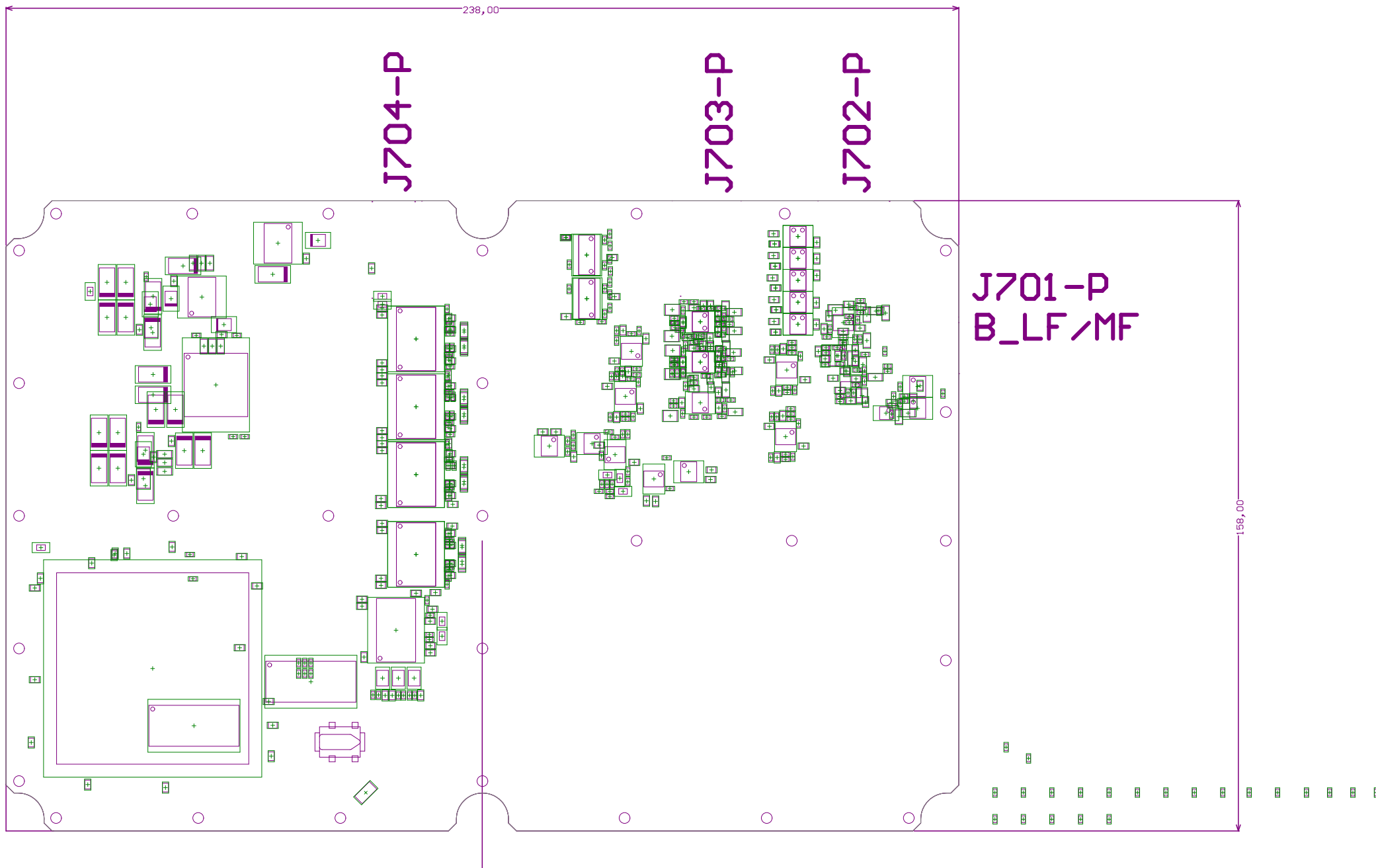
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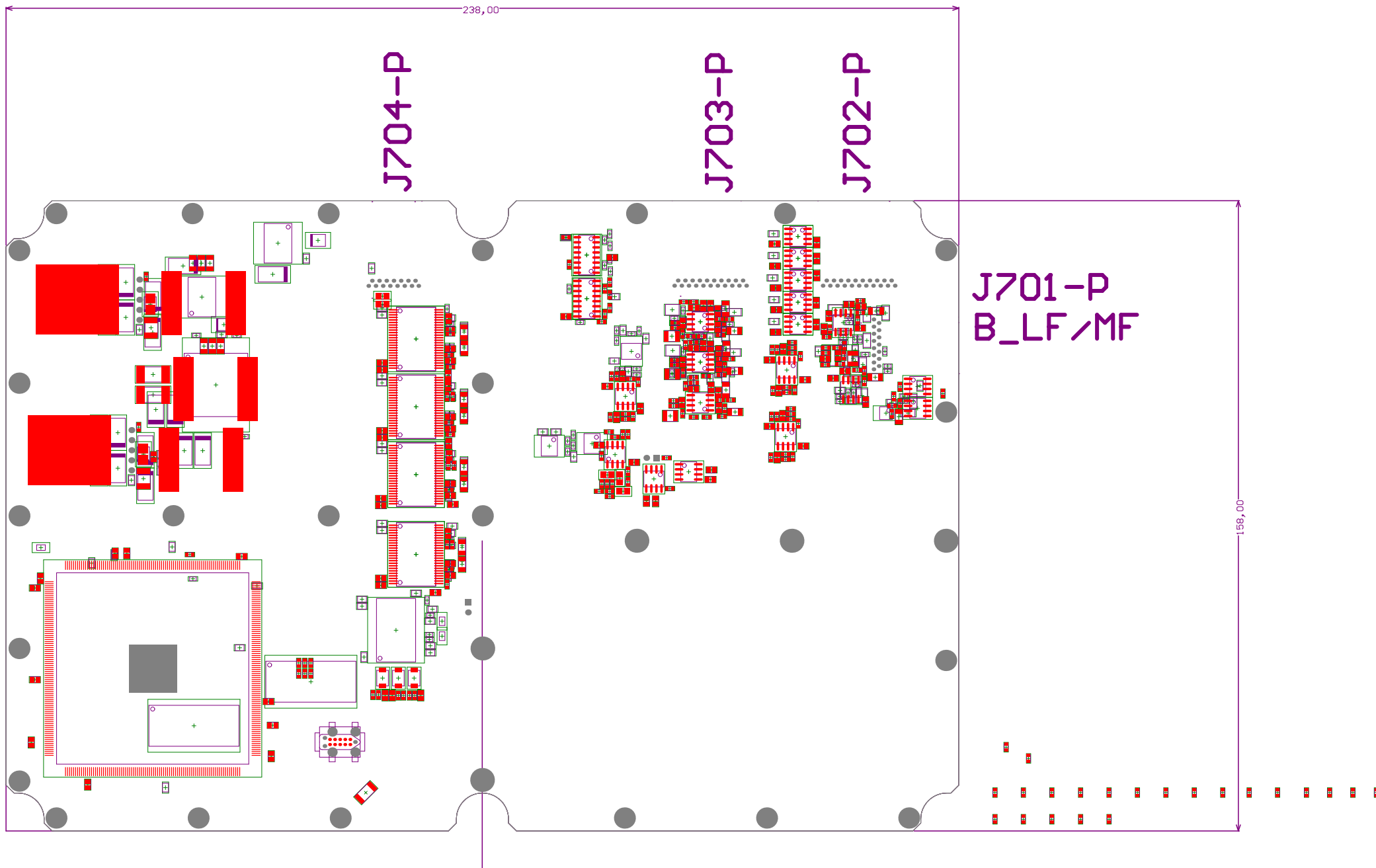


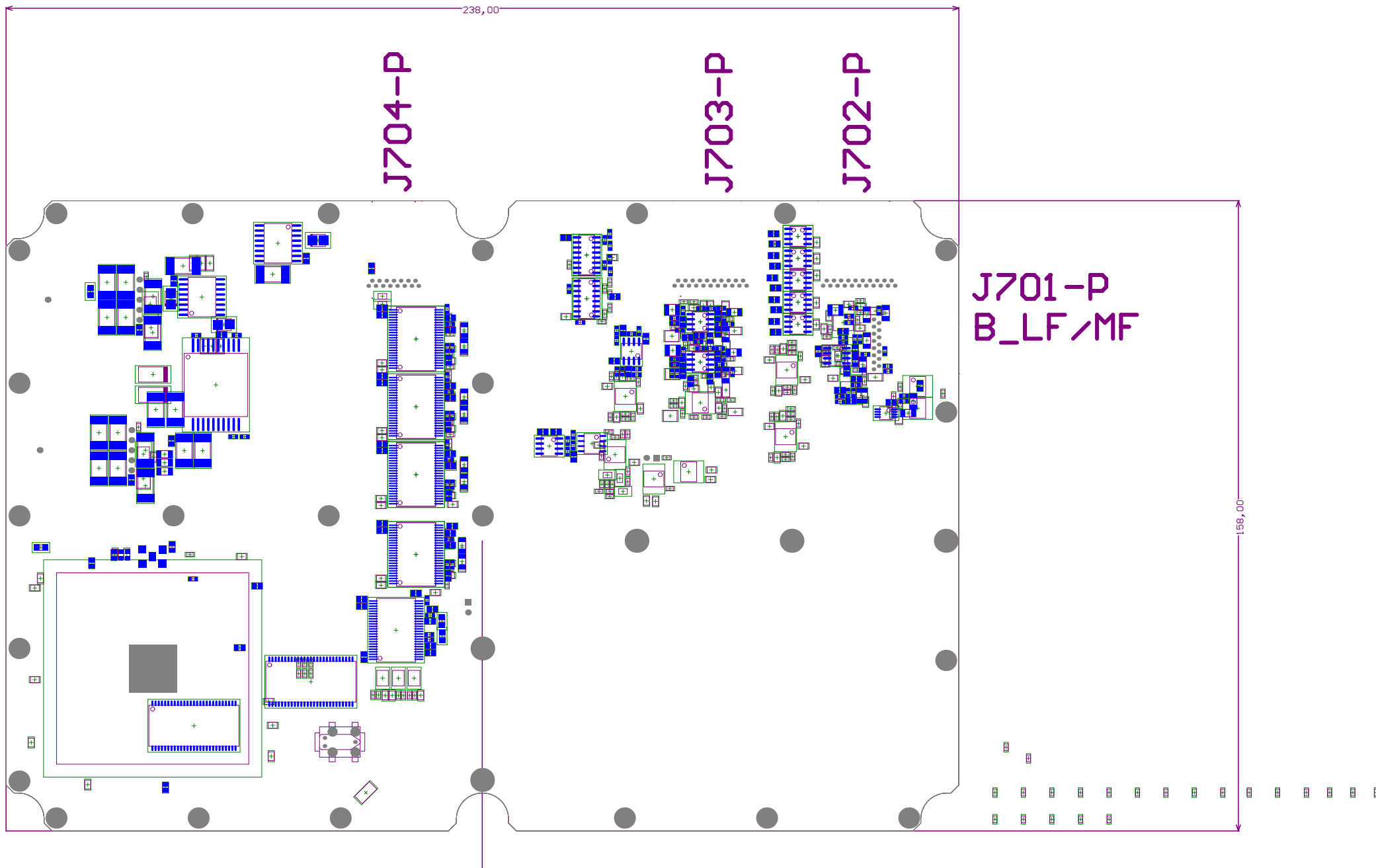


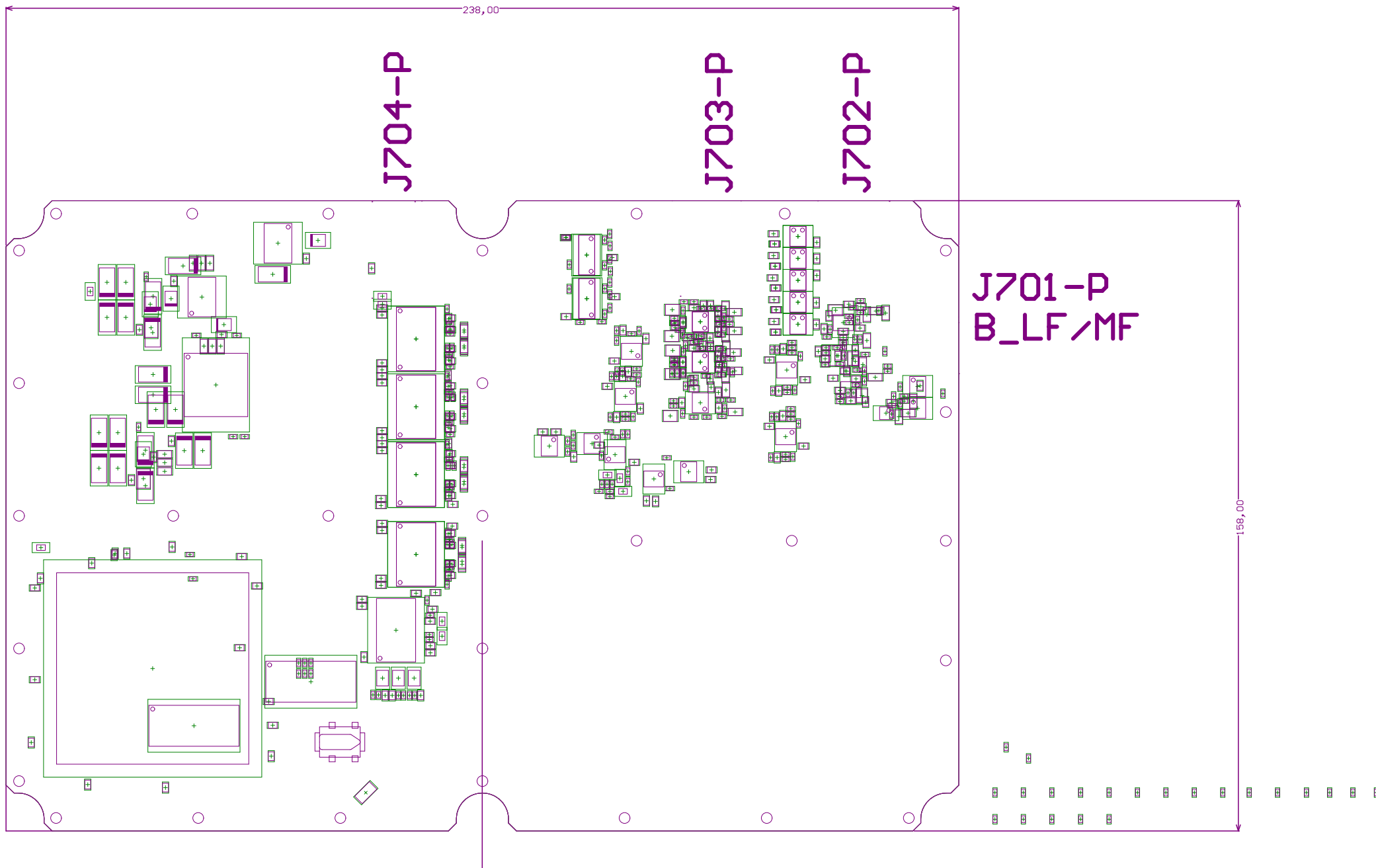


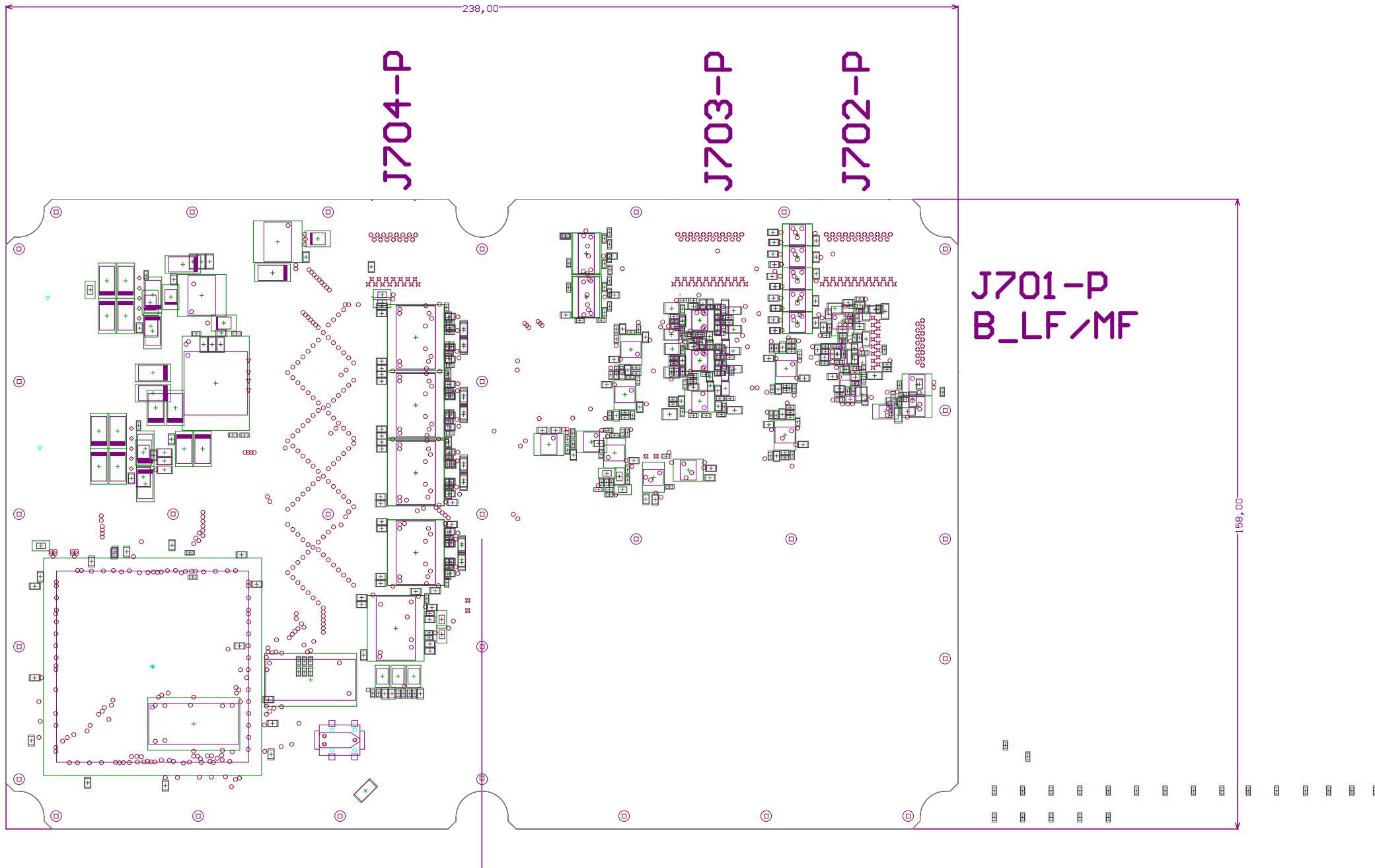


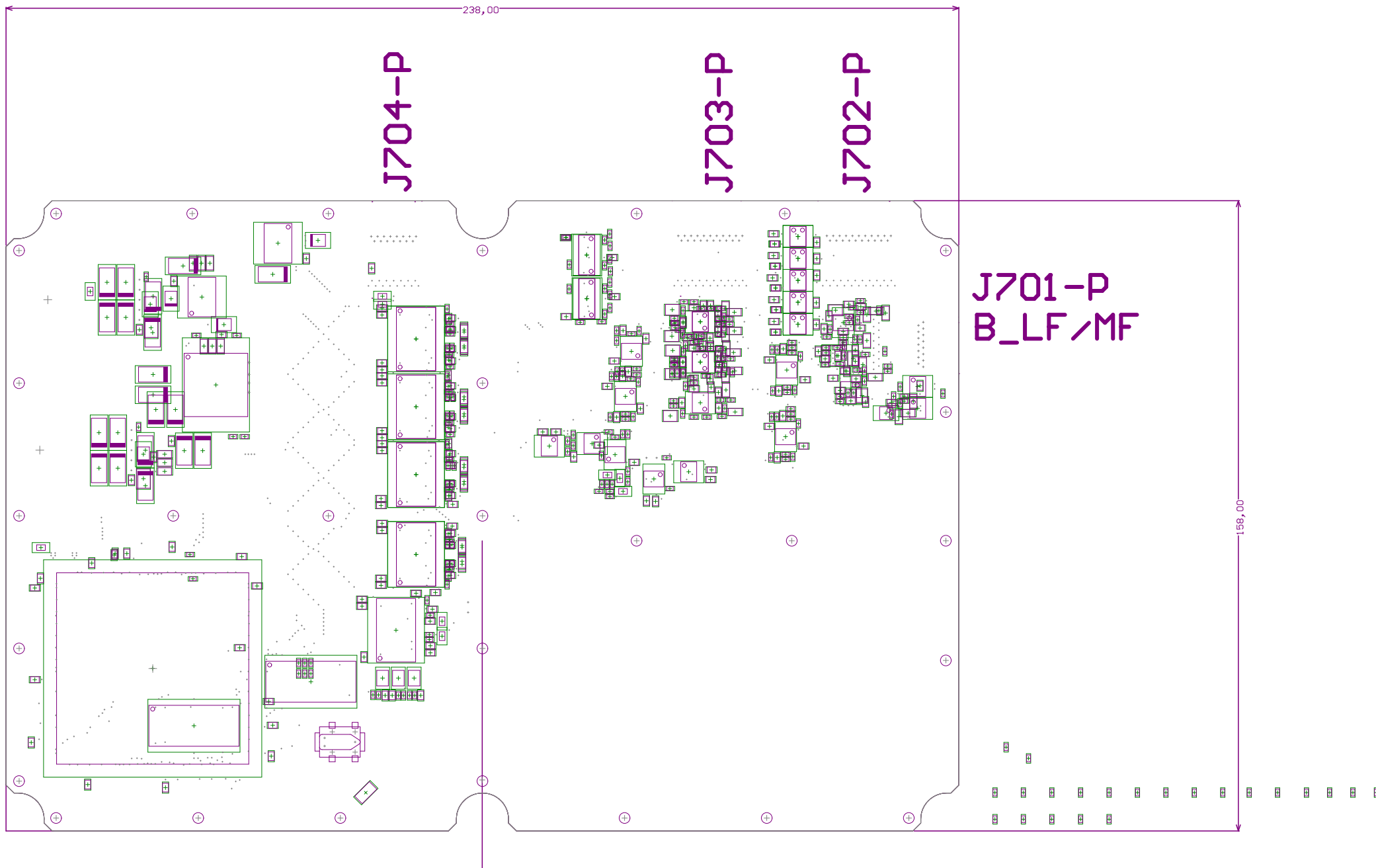












[illegible]