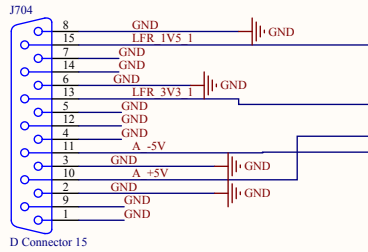
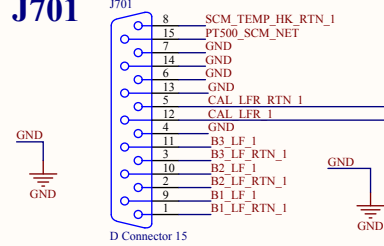


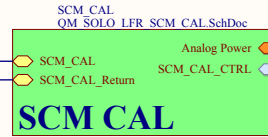
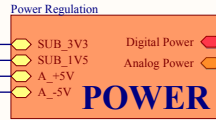
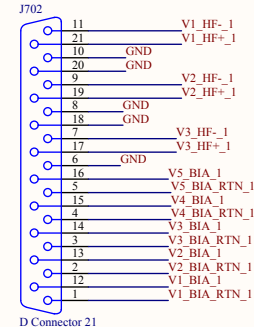
J704



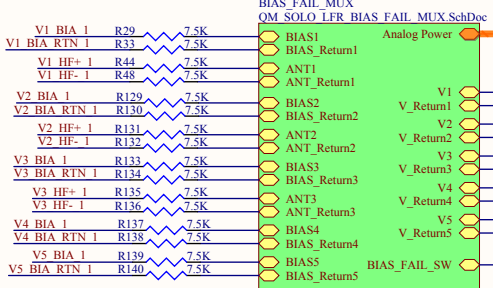
J701



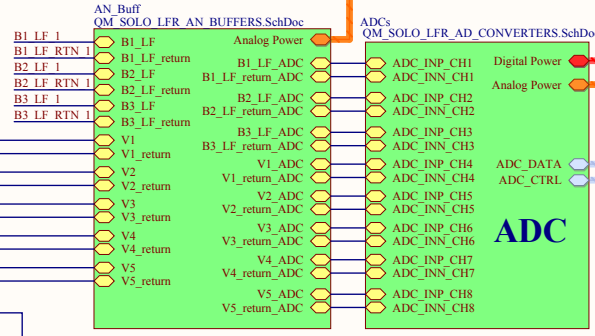
J702



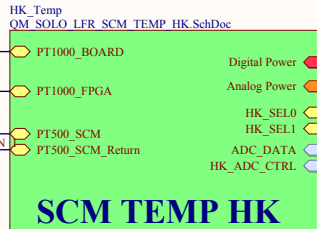
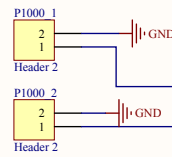
BIAS FAIL MUX



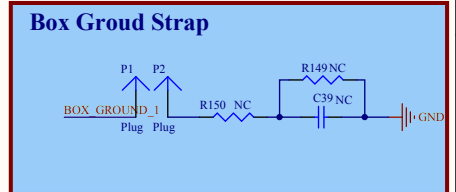
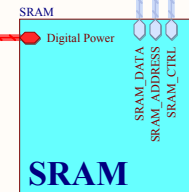
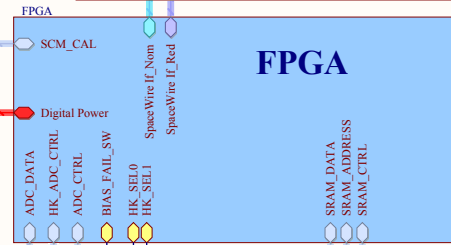
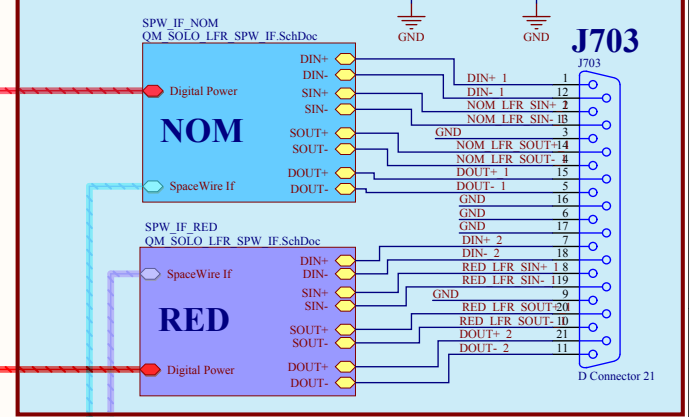
AN BUFFERS



BIAS FAIL SW



SPACEWIRE



CHANGELOG
QM_CHANGELOG.SchDoc

CHANGELOG

Title	LFM QM TOP	Author	Alexis Jeandet
Size:	A3	Number:	LFM-172200-EM
Date:	02/05/2014	Time:	08:36:56
Contact:	alexis.jeandet@lpp.polytechnique.fr		
File:	F:\Missions/Satellites/SolarOrbiter/LFR/PCB/QM/QM_SOLO_LFR_TOP.SchDoc		



CHANGELOG

09/04/2014

- Moved analog input buffers resistors before the swithes.
- C21 (100nF cap @ SUB1.5V input) footprint changed to 0805.
- Connected SENS input for RHFL4913 to Vout.
- 2.5V analogic connected to sub 3.3V.
- added R/C Slow start on 2.5V RHFL4913.
- 1.8V MSK5822 VBias input moved from 5V to sub 3.3V.

14/04/2014

- Connected SCM cal and SPW shield to GND.
- Unconnected Pin are connected to Unconnected Net which is tied to GND.

15/04/2014

- Updated ground strap, it's now removable and the circuit is a R C//R.

22/04/2014


- Connected 3.3V regulator VBIAS input to sub 3.3V.
- Connected MSKs Latch input to GND.
- Connected RHFL4913 INH inputs to GND.
- Replaced DG419 with 54HC4053 for bais/ant mux.

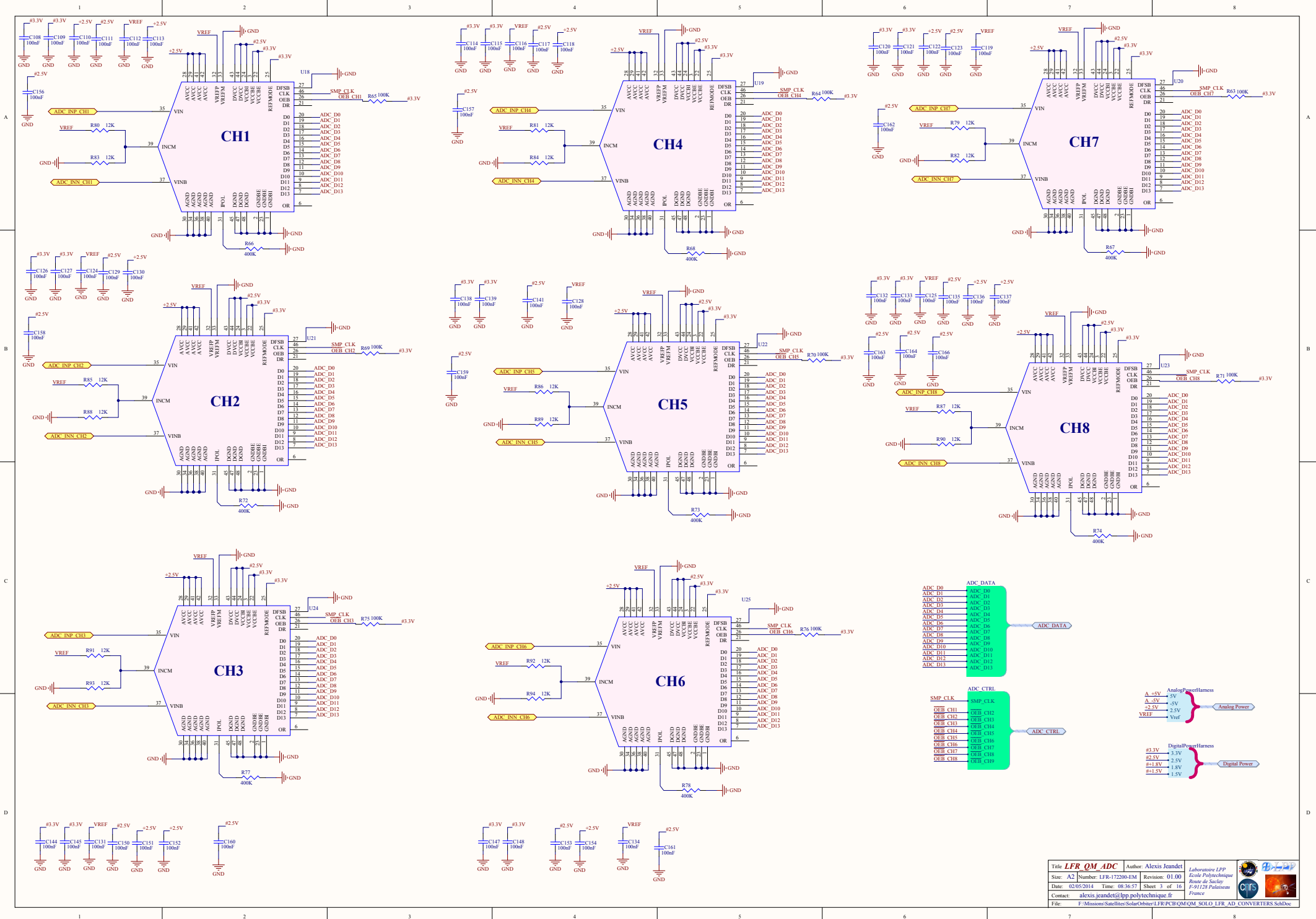
24/04/2014

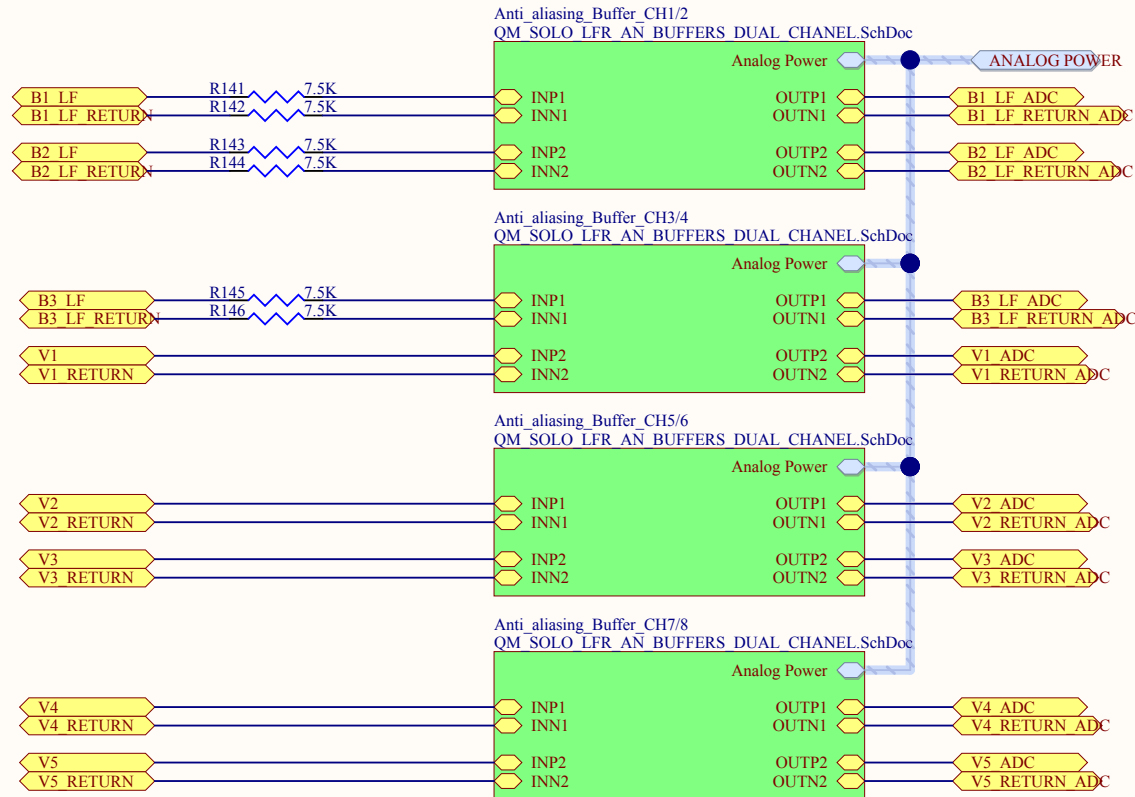
- Replaced EM SRAM with FM SRAM UT8ER1M32.

30/04/2014

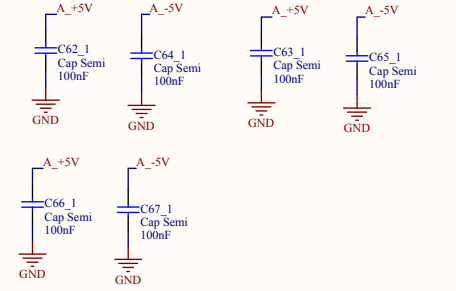
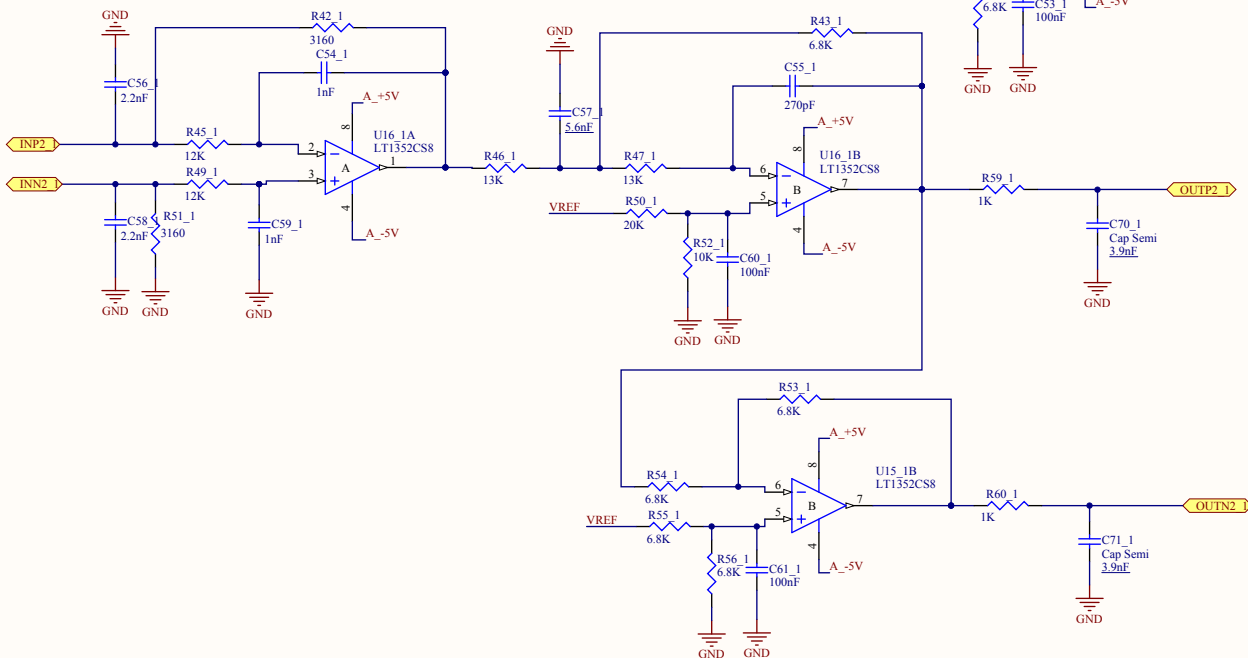
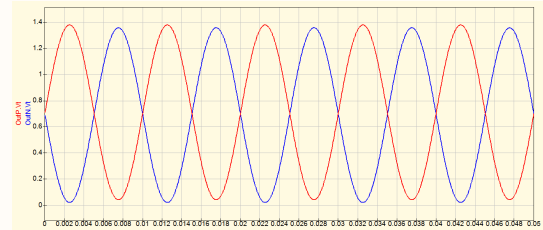
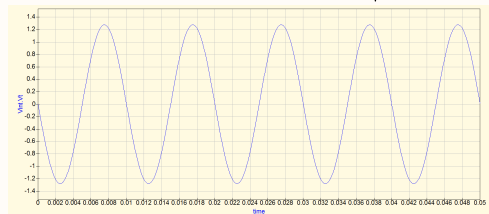
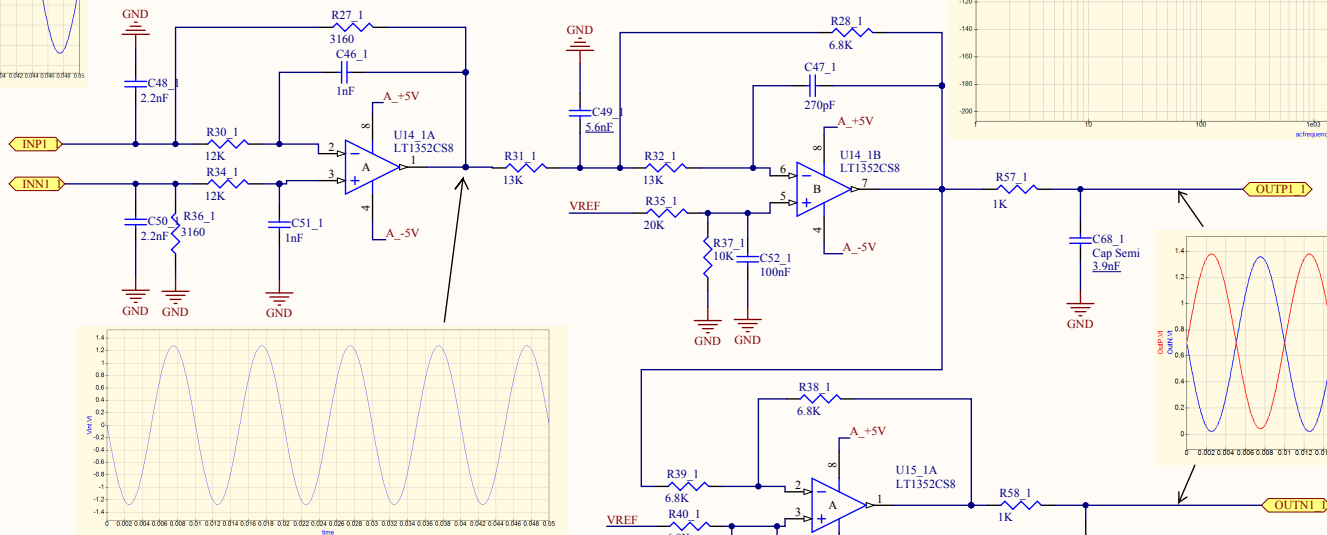
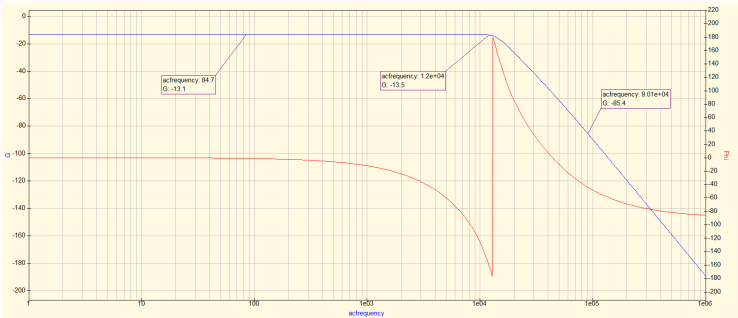
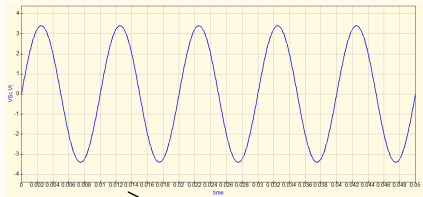
- Replaced EM Oscillators with FM.
- Replaced EM HK DAC with FM.

Title CHANGELOG		Author: Alexis Jeandet		
Size: A4	Number: LFR-172200-EM	Revision: 01.00		
Date: 02/05/2014	Time: 08:36:56	Sheet 2 of 16		
Contact: alexis.jeandet@lpp.polytechnique.fr				
File: F:\Missions\Satellites\SolarOrbiter\LFR\PCB\QM\QM_CHANGELOG.SchDoc				



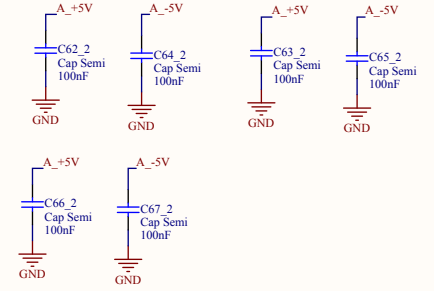
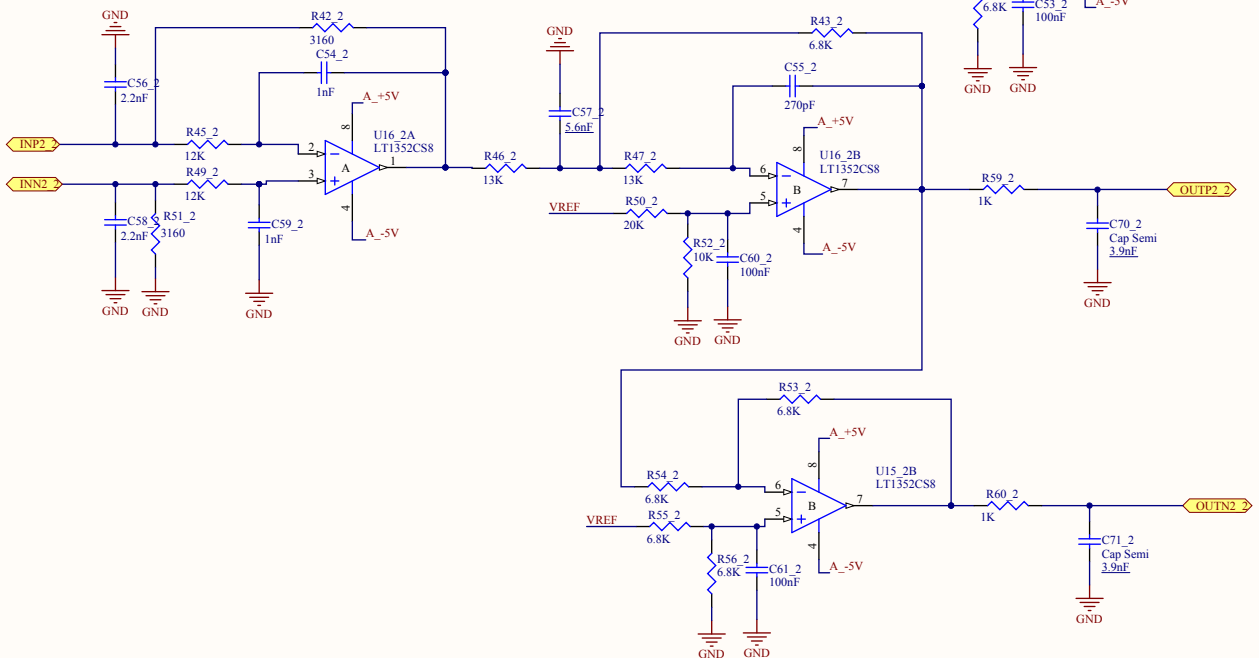
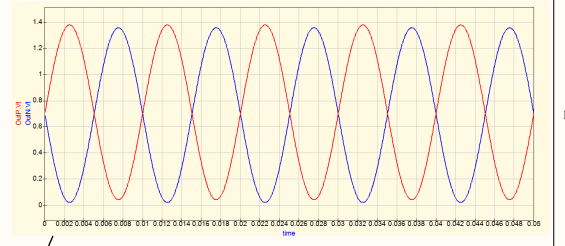
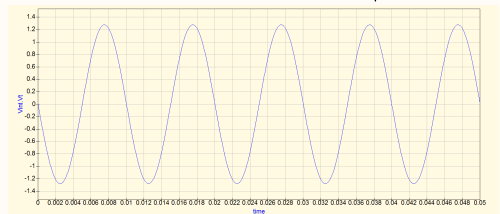
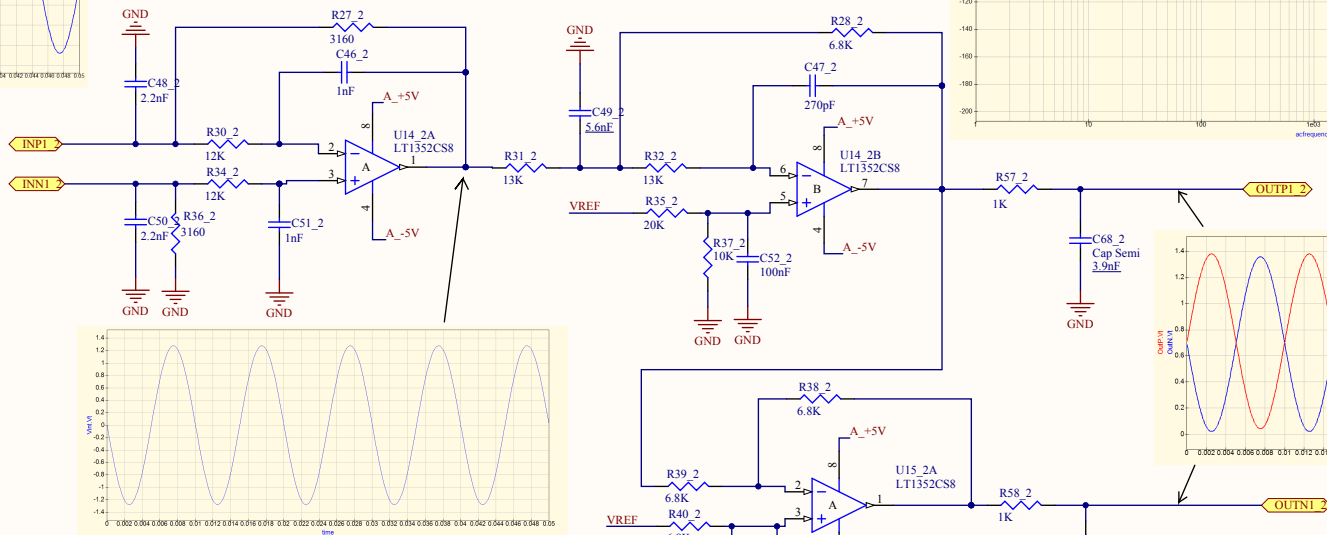
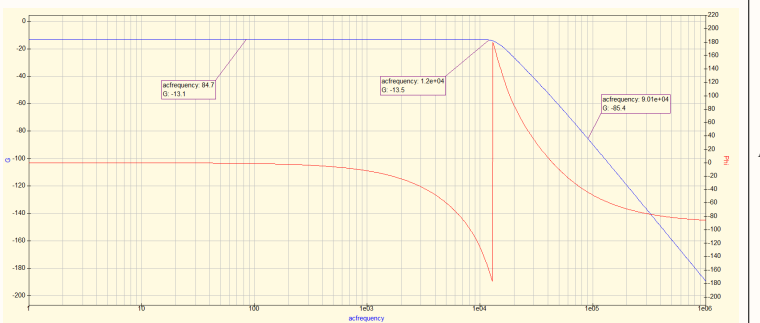
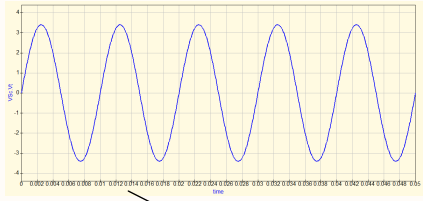


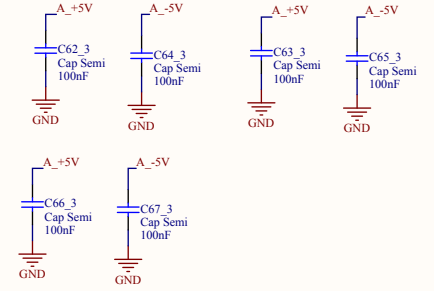
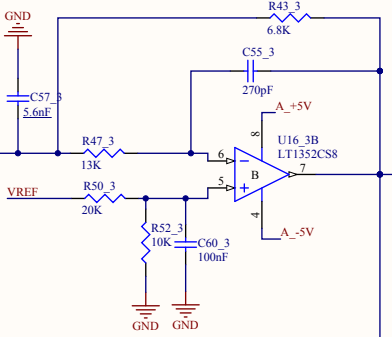
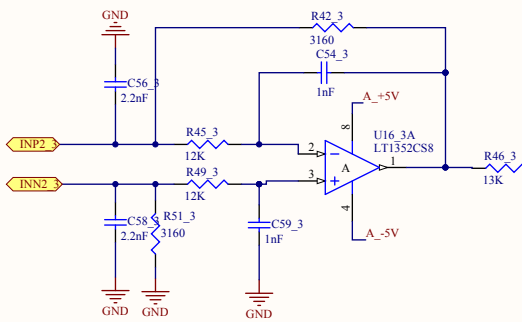
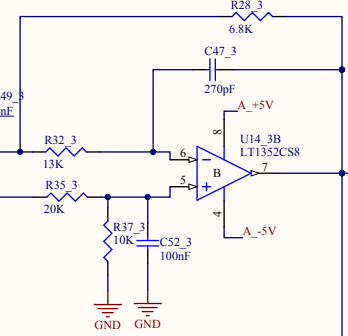
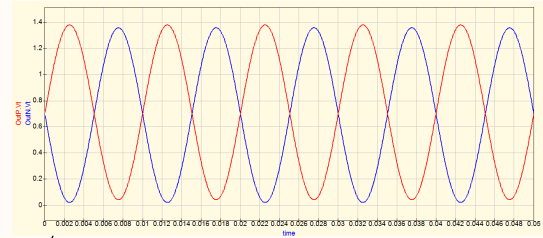
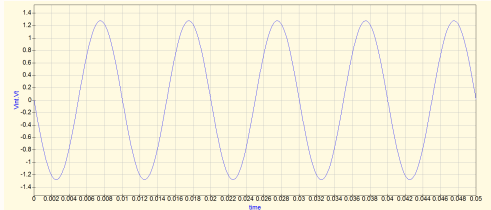
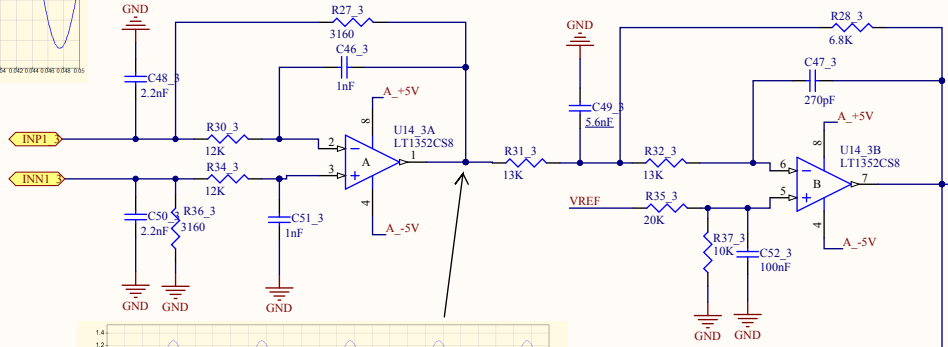
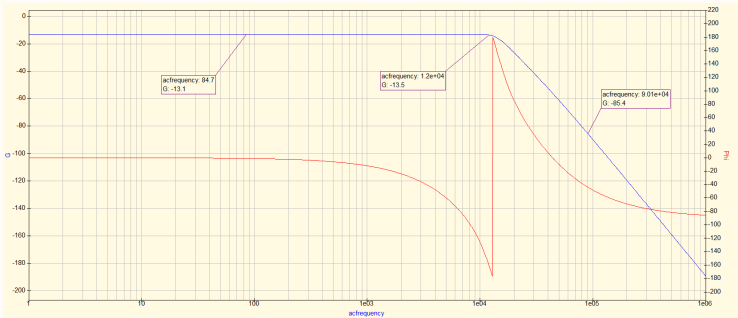
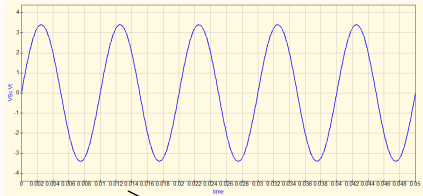
Title LFR_QM_AN		Author: Alexis Jeandet		Laboratoire LPP Ecole Polytechnique Route de Saclay F-91128 Palaiseau France	
Size: A4	Number: LFR-172200-EM	Revision: 01.00			
Date: 02/05/2014	Time: 08:36:57	Sheet 4 of 16			
Contact: alexis.jeandet@lpp.polytechnique.fr					
File: F:\Missions\Satellites\SolarOrbiter\LFR\PCB\QM\QM_SOLO_LFR_AN_BUFFERS.SchDoc					

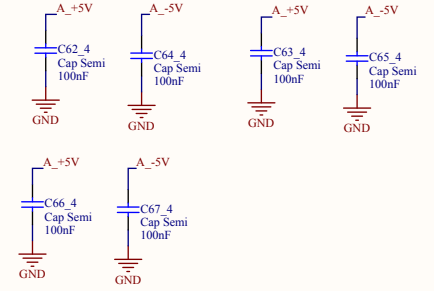
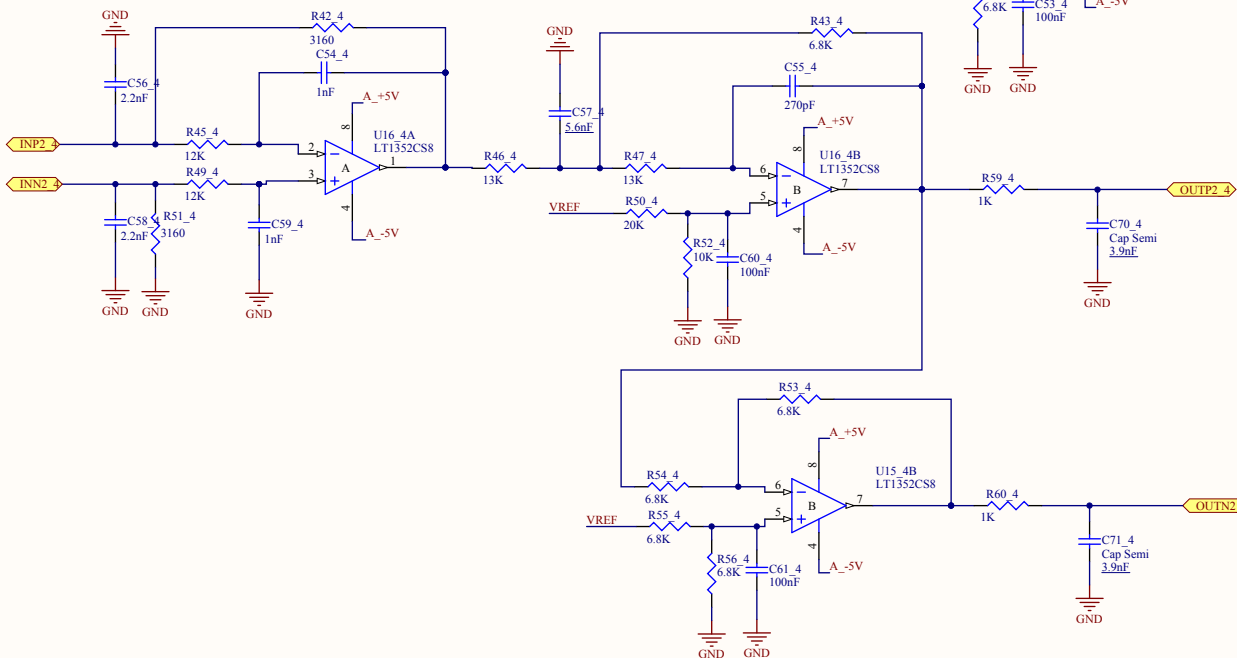
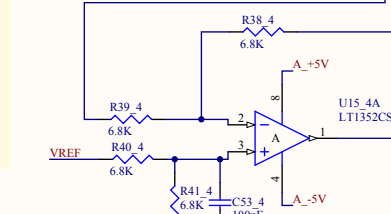
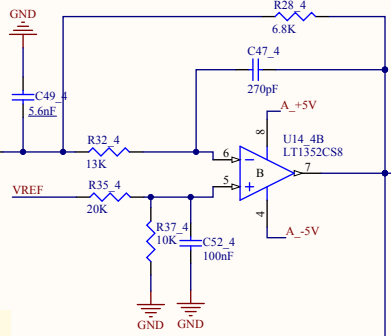
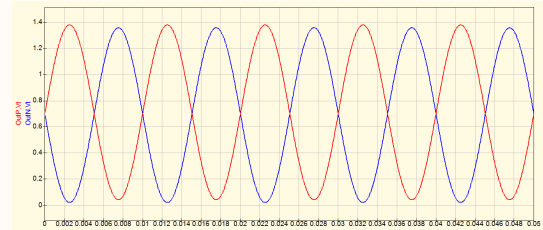
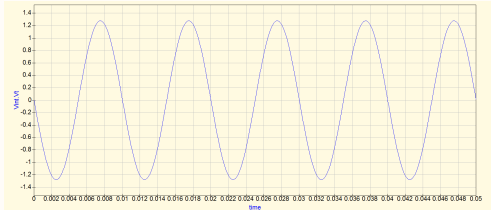
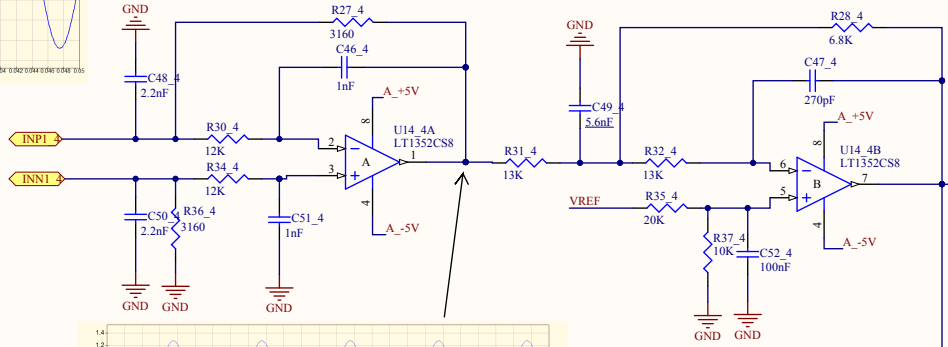
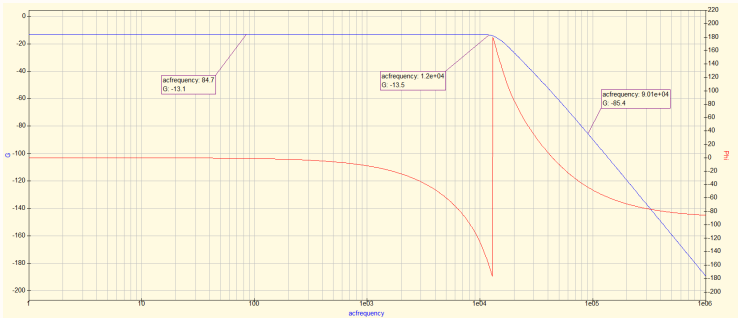
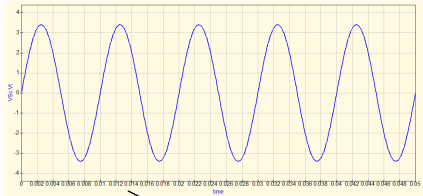


Title	LFR_QM_BUFF	Author:	Alexis Jeandet
Size:	A3	Number:	LFR-172200-EM
Date:	02/05/2014	Time:	08:36:57
Contact:	alexis.jeandet@lpp.polytechnique.fr		
File:	F:\Missions\Satellites\SolarOrbiter\LFR\PCB\QM\SOLO_LFR_AN_BUFFERS_DUAL_CHANNEL_Sch.Doc		

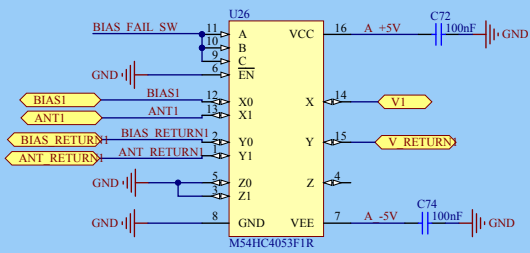




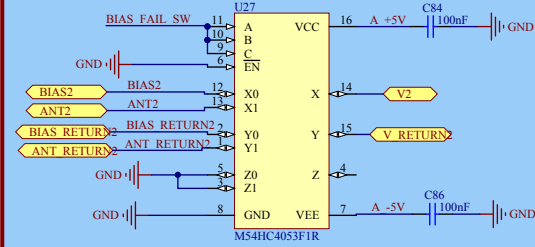




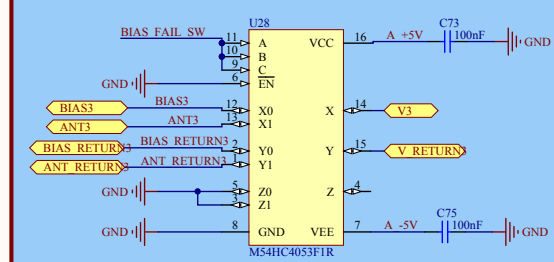
BIAS1/ANT1 Channel



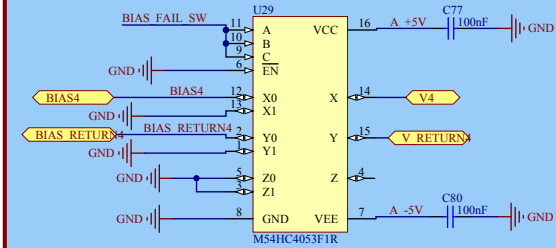
BIAS2/ANT2 Channel



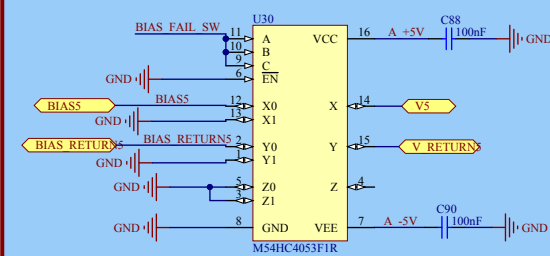
BIAS3/ANT3 Channel



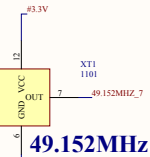
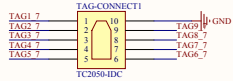
BIAS4 Channel



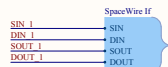
BIAS5 Channel



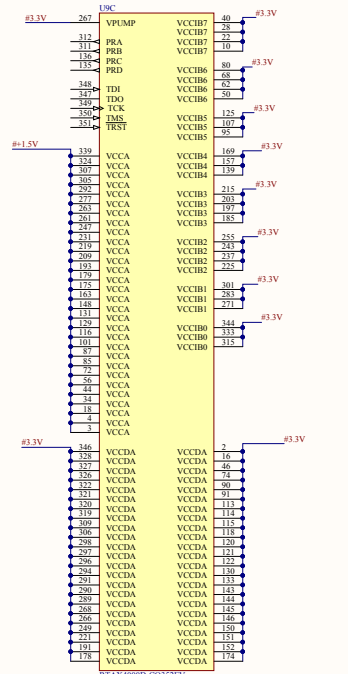
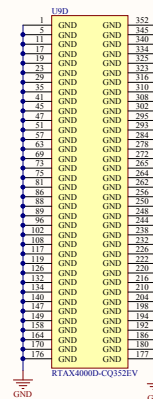
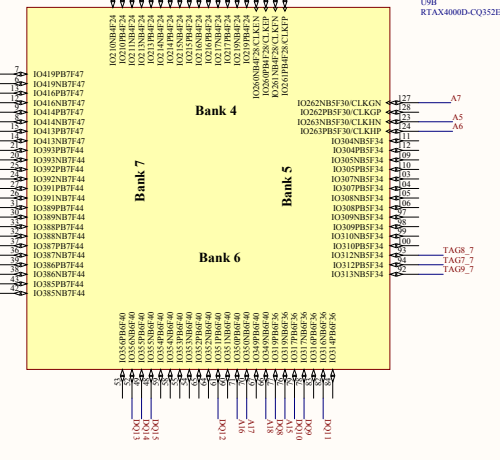
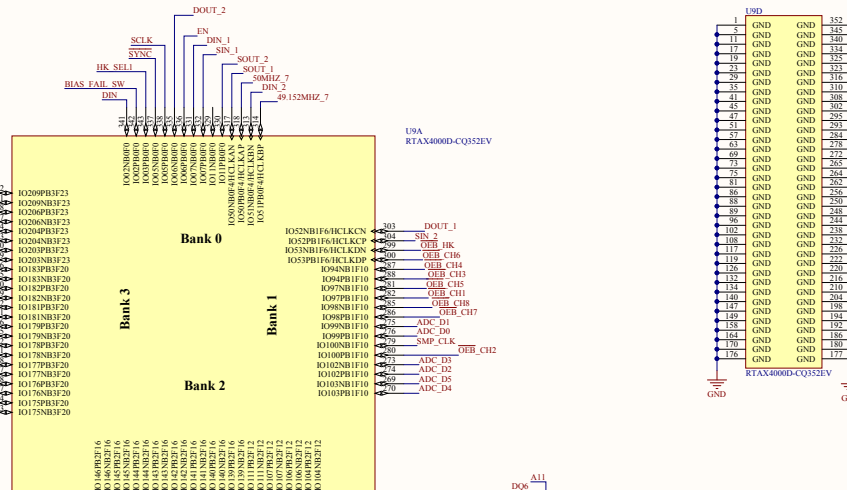
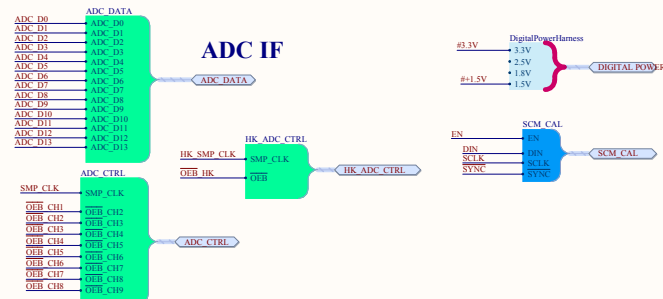
TAG-Probe



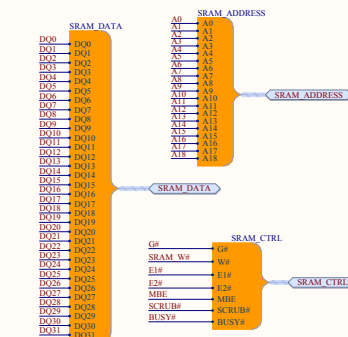
49.152MHz
QM&FM @50MHz
BBM,DM&EM @100MHz



ADC IF



SRAM IF



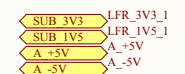
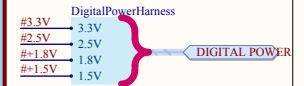
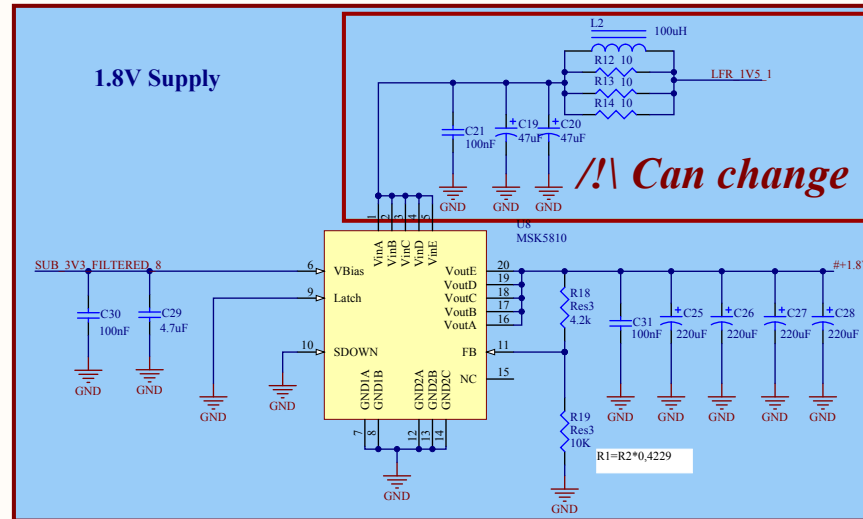
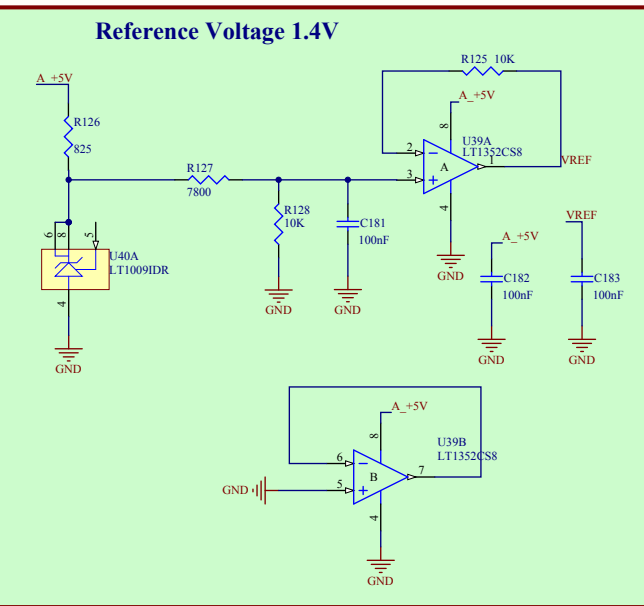
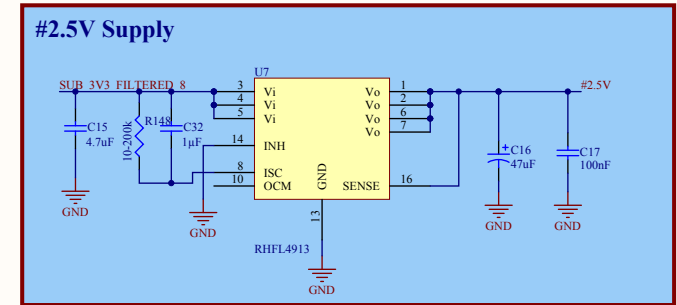
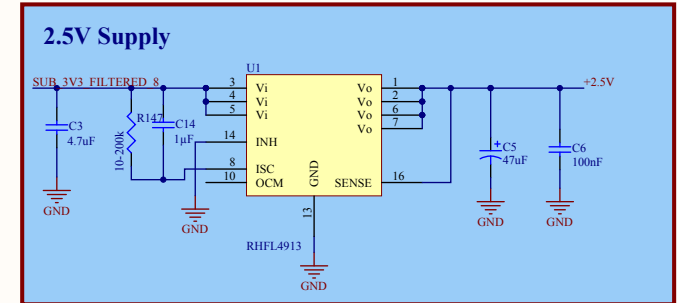
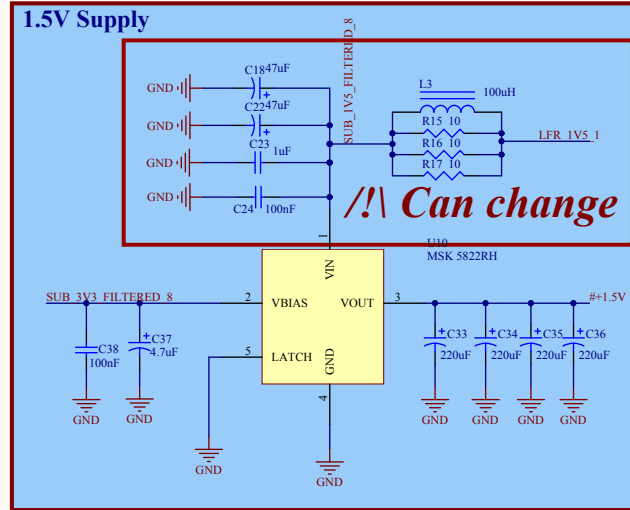
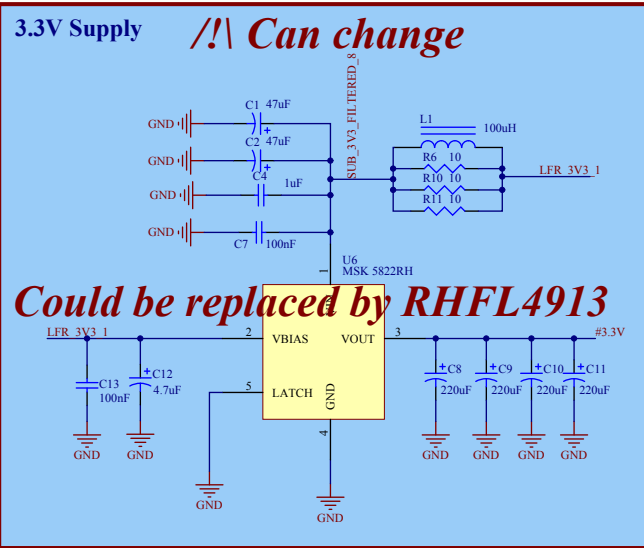
Characterization

Power-Up Characterization

Power supplies for the RTAX-S/SL devices can power up in any sequence. Figure 1 and Figure 2 show the power-up characteristics for the different sequencing between VCCA (1.5 V) and VCCDA/VCCIBX (3.3 V). No significant transient current (>5 mA) is observed with either sequence.

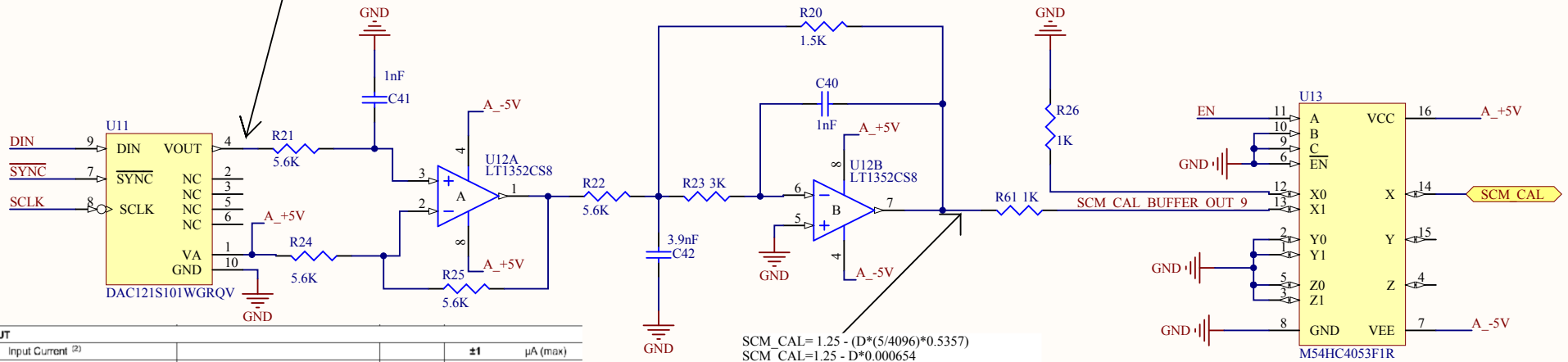
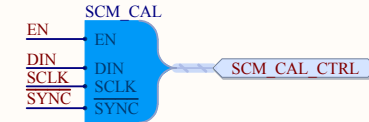
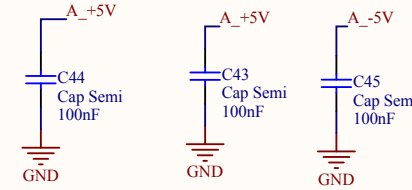
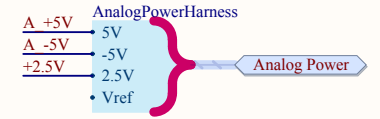
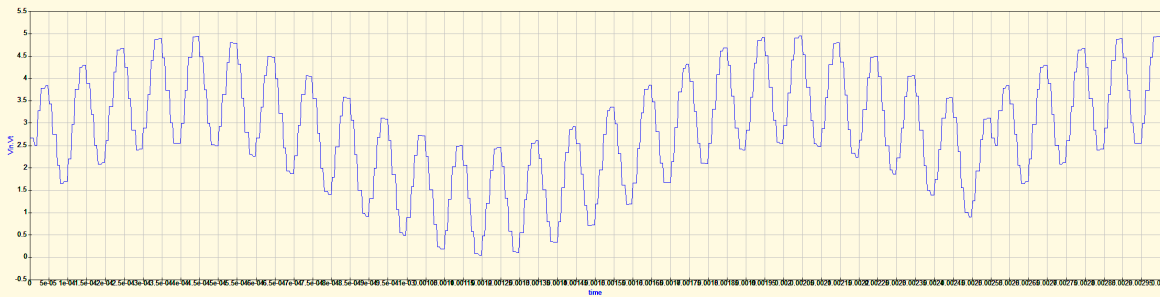
Uses Rev H for MSK5822 and MSK5810 regulators documentation!

220uF => TAZ-H package
47uF => TAZ-H package
4.7uF => TAJ-B package



REQ-RPW-LFR-4706 LFR shall deliver a calibration signal to the SCM. This signal will be the sum of two sinus waves, at different frequencies $f_1 = 625$ Hz and $f_2 = 10$ kHz, with amplitudes of 500 mVpp, a sampling frequency of [TBD], a resolution of 8 bits and a duration of 4 s.

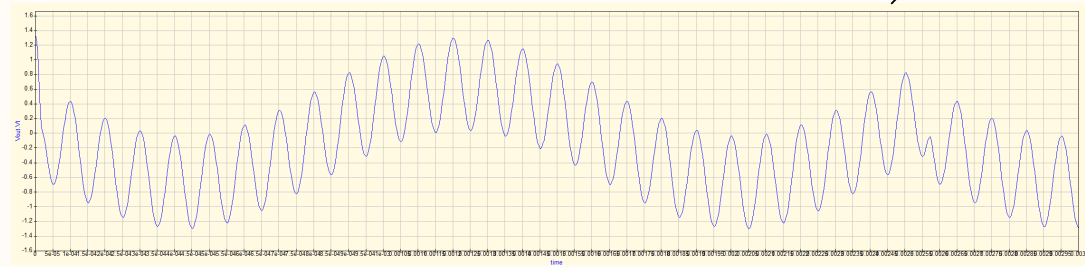
When not used, the calibration signal will be tied to ground (TBC) via an analog switch.



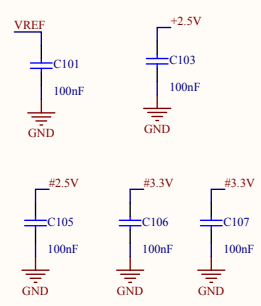
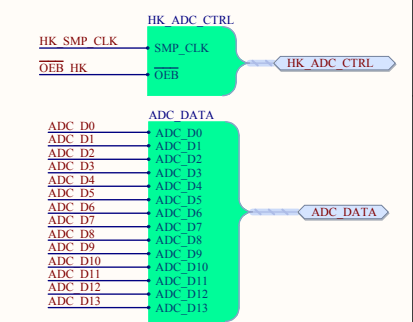
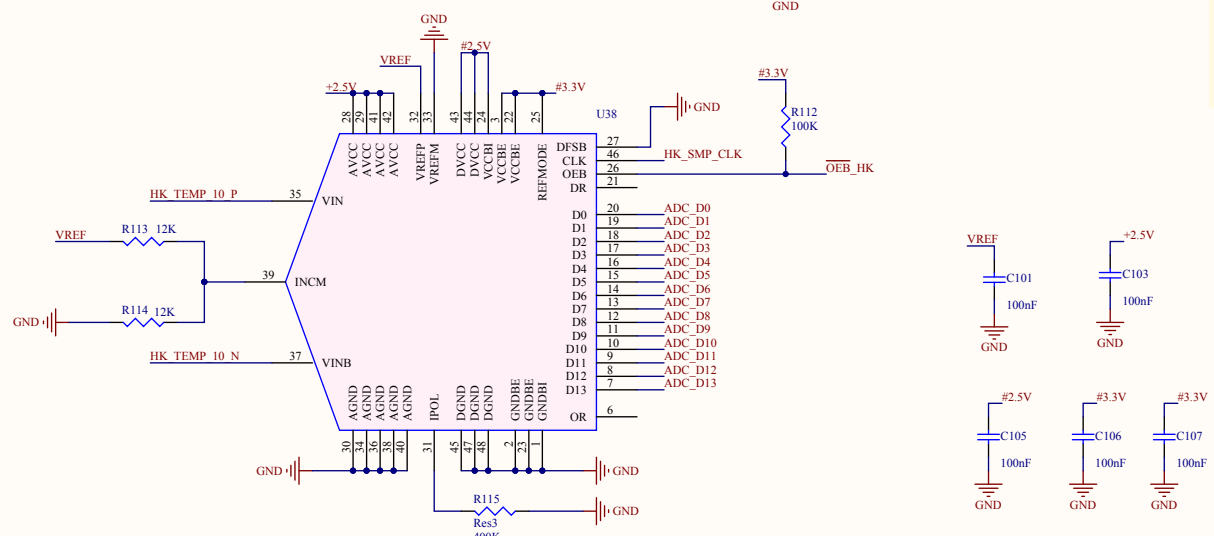
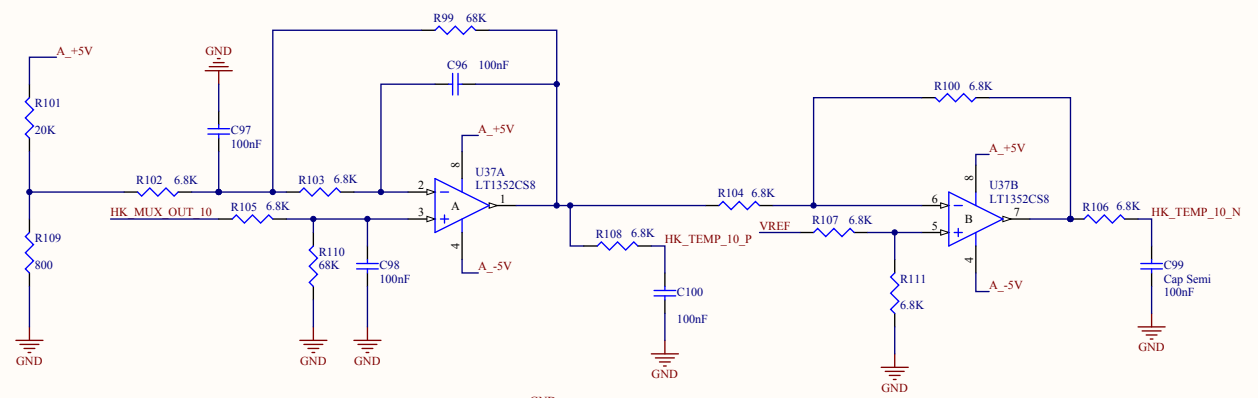
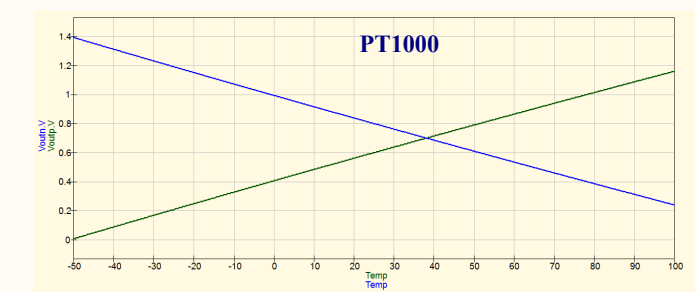
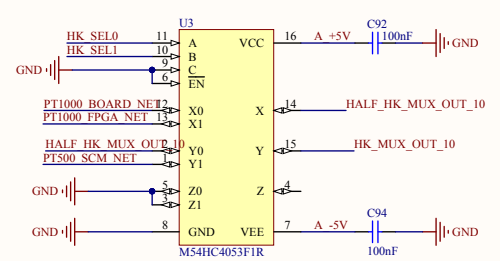
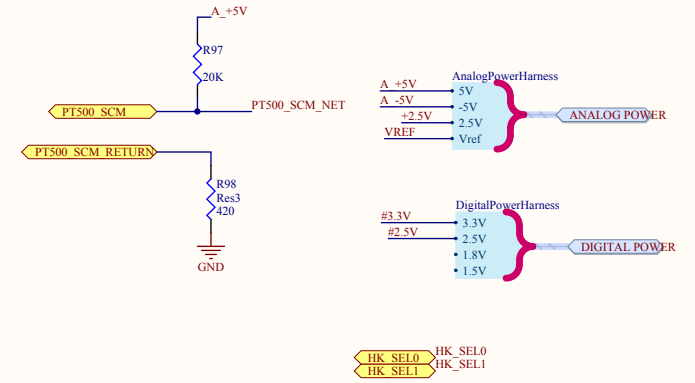
$$SCM_CAL = 1.25 - (D * (5/4096) * 0.5357)$$

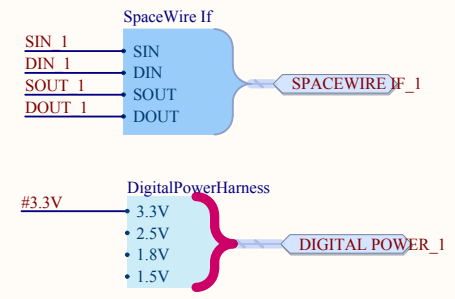
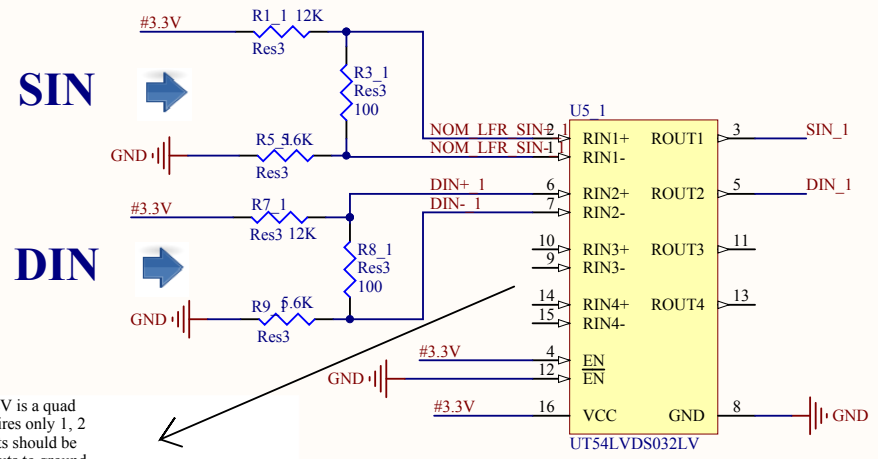
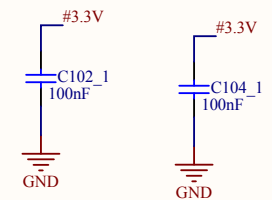
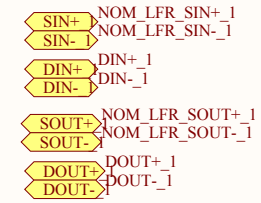
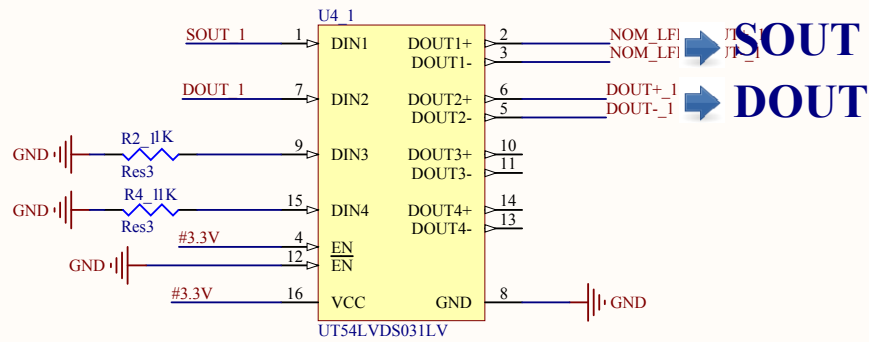
$$SCM_CAL = 1.25 - D * 0.000654$$

LOGIC INPUT			
I_{IH}	Input Current ⁽²⁾	± 1	μA (max)
V_{IL}	Input Low Voltage ⁽²⁾	$V_A = 5V$ $V_A = 3V$	0.8 V (max) 0.5 V (max)
V_{HI}	Input High Voltage ⁽²⁾	$V_A = 5V$ $V_A = 3V$	2.4 V (min) 2.1 V (min)
C_{IN}	Input Capacitance ⁽²⁾	3	pF (max)



Title	LFR_QM_CAL	Author:	Alexis Jeandet	
Size:	A4	Number:	LFR-172200-EM	
Date:	02/05/2014	Time:	08:36:59	
Contact:	alexis.jeandet@lpp.polytechnique.fr			
File:	F:\Missions\Satellites\SolarOrbiter\LFR\PCB\QM\QM_SOLO_LFR_SCM_CAL.SchDoc			
Revision:	01.00	Sheet	9 of 16	

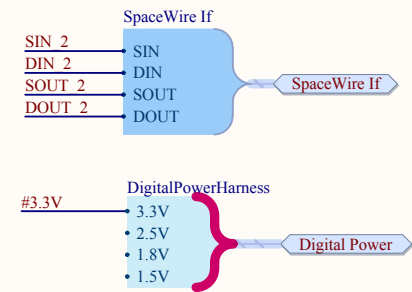
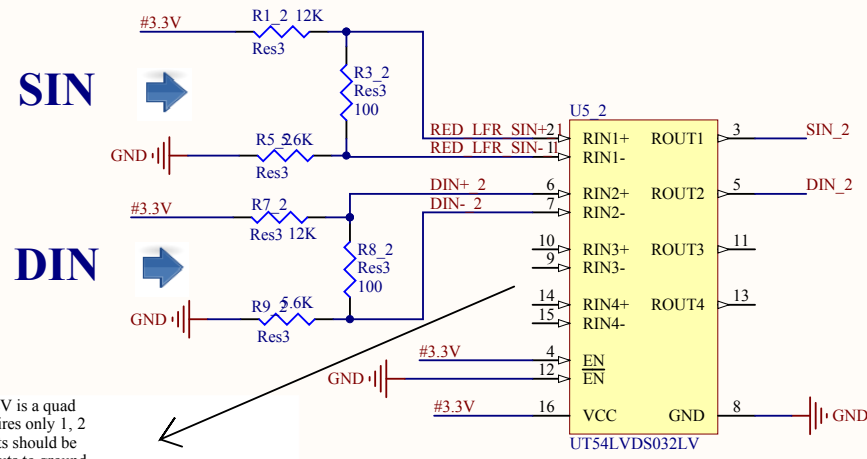
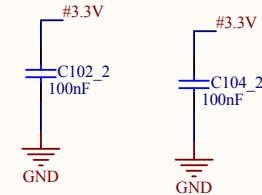
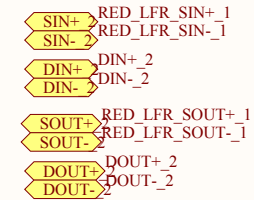
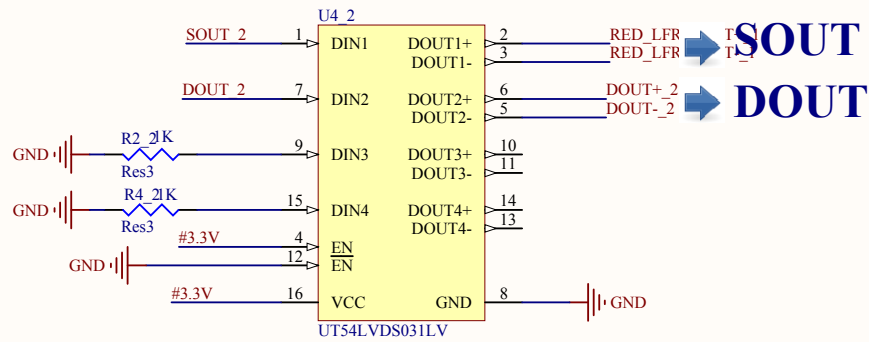




1. Open Input Pins. The UT54LVDS032LV is a quad receiver device, and if an application requires only 1, 2 or 3 receivers, the unused channel(s) inputs should be left OPEN. Do not tie the unused receiver inputs to ground or any other voltages. The input is biased by internal high value pull up and pull down resistors to set the output to a HIGH state. This internal circuitry will guarantee a HIGH, stable output state for open inputs.

cf : <http://www.aeroflex.com/ams/pagesproduct/datasheets/LVDSReceiver3v.pdf>

Title	LFR_QM_SPW	Author:	Alexis Jeandet		
Size:	A4	Number:	LFR-172200-EM		
Date:	02/05/2014	Time:	08:36:59	Revision:	01.00
Contact:	alexis.jeandet@lpp.polytechnique.fr			Sheet	11.bf 16
File:	F:\Missions\Satellites\SolarOrbiter\LFR\PCB\QM\QM_SOLO_LFR_SPW_IF.SchDoc				

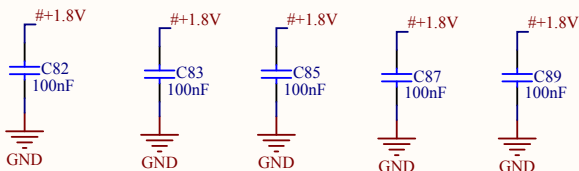
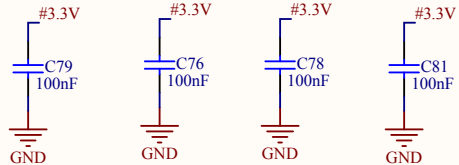
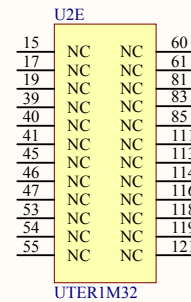
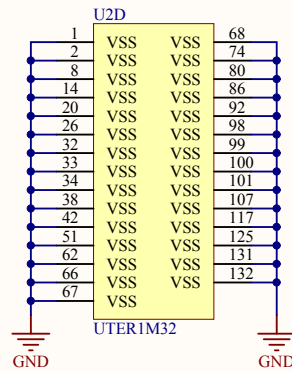
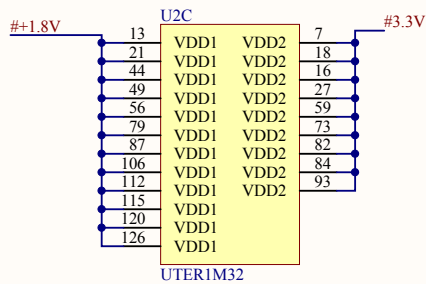
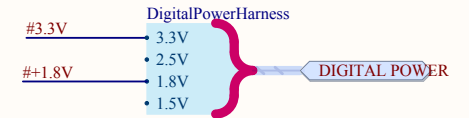
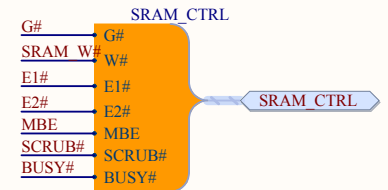
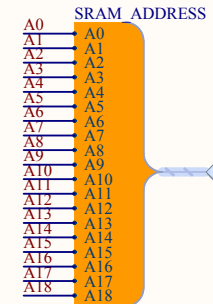
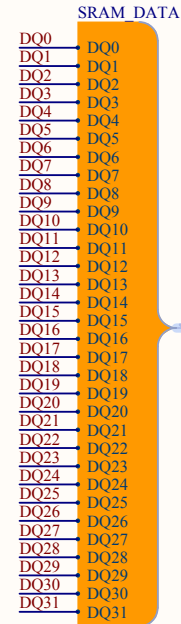
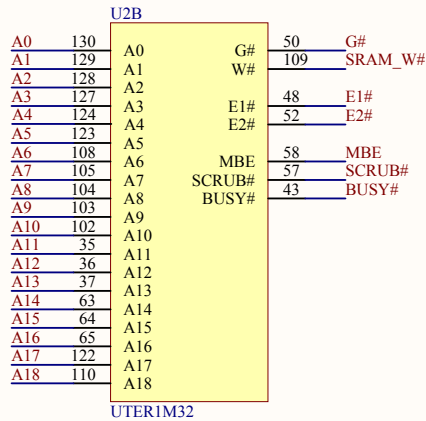
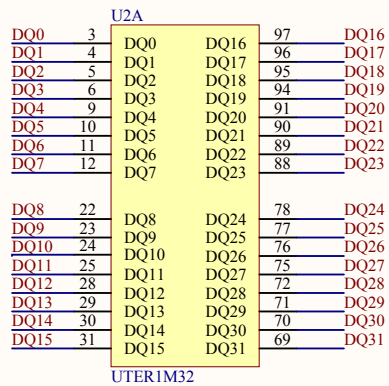


1. Open Input Pins. The UT54LVDS032LV is a quad receiver device, and if an application requires only 1, 2 or 3 receivers, the unused channel(s) inputs should be left OPEN. Do not tie the unused receiver inputs to ground or any other voltages. The input is biased by internal high value pull up and pull down resistors to set the output to a HIGH state. This internal circuitry will guarantee a HIGH, stable output state for open inputs.

cf : <http://www.aeroflex.com/ams/pagesproduct/datasheets/LVDSReceiver3v.pdf>



Title LFR_QM_SPW		Author: Alexis Jeandet	
Size: A4	Number: LFR-172200-EM	Revision: 01.00	
Date: 02/05/2014	Time: 08:36:59	Sheet 11.2f 16	
Contact: alexis.jeandet@lpp.polytechnique.fr			
File: F:\Missions\Satellites\SolarOrbiter\LFR\PCB\QM\QM_SOLO_LFR_SPW_IF.SchDoc			

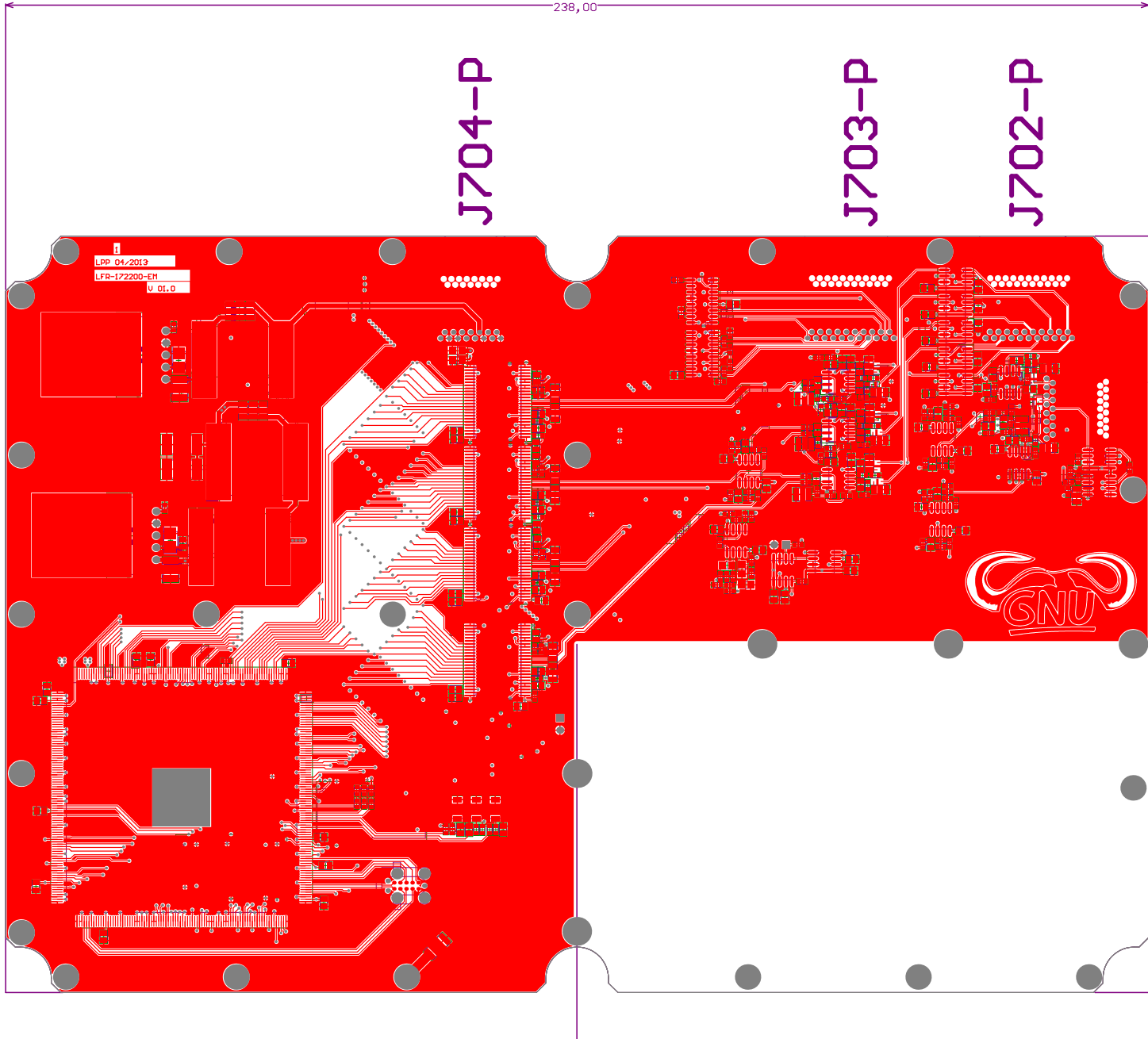




Title	LFR_QM_SRAM	Author:	Alexis Jeandet
Size:	A4	Number:	LFR-172200-EM
		Revision:	01.00
Date:	02/05/2014	Time:	08:37:00
		Sheet	12 of 16
Contact:	alexis.jeandet@lpp.polytechnique.fr		
File:	F:\Missions\Satellites\SolarOrbiter\LFR\PCB\QM\QM_SOLO_LFR_SRAM.SchDoc		

Laboratoire LPP
Ecole Polytechnique
Route de Saclay
F-91128 Palaiseau
France

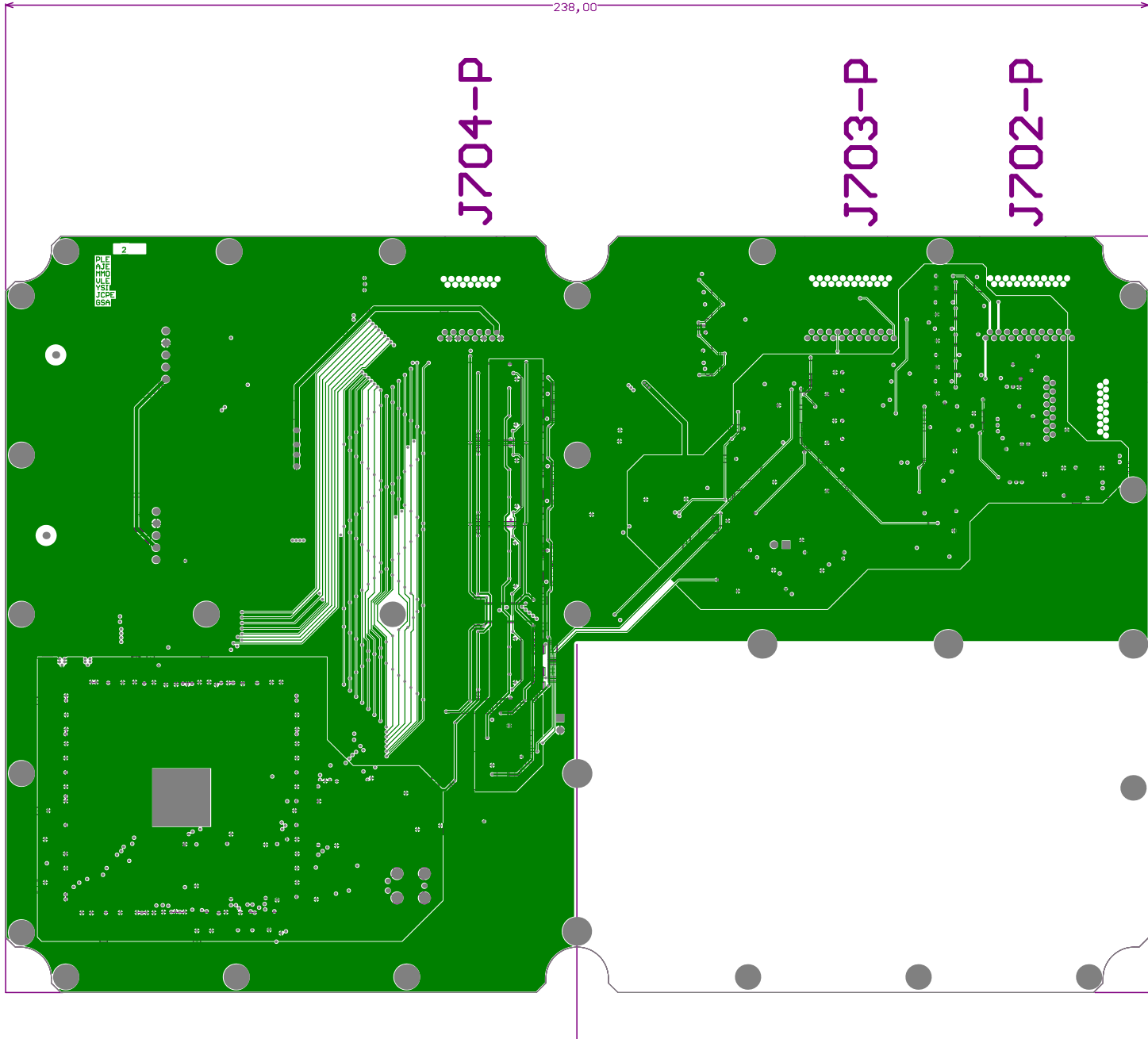
J704-P

J703-P

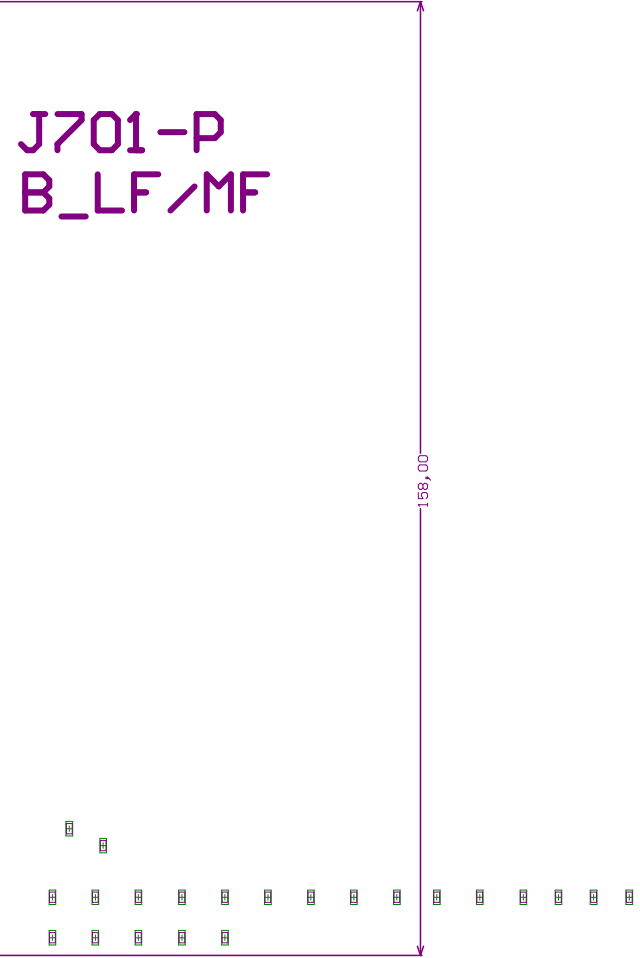
J702-P

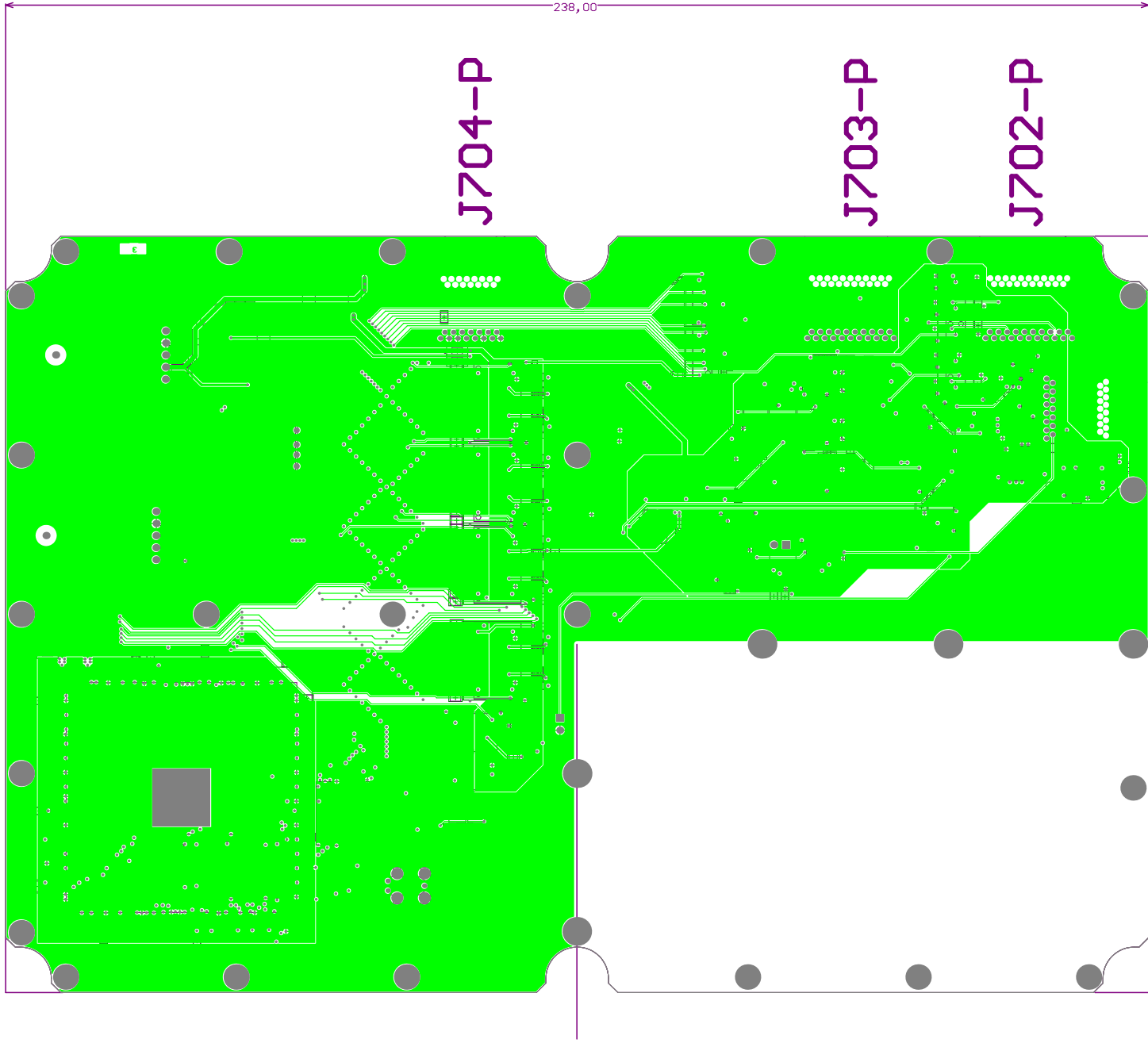
J701-P
B_LF/MF

158,00



J701-P
B_LF/MF

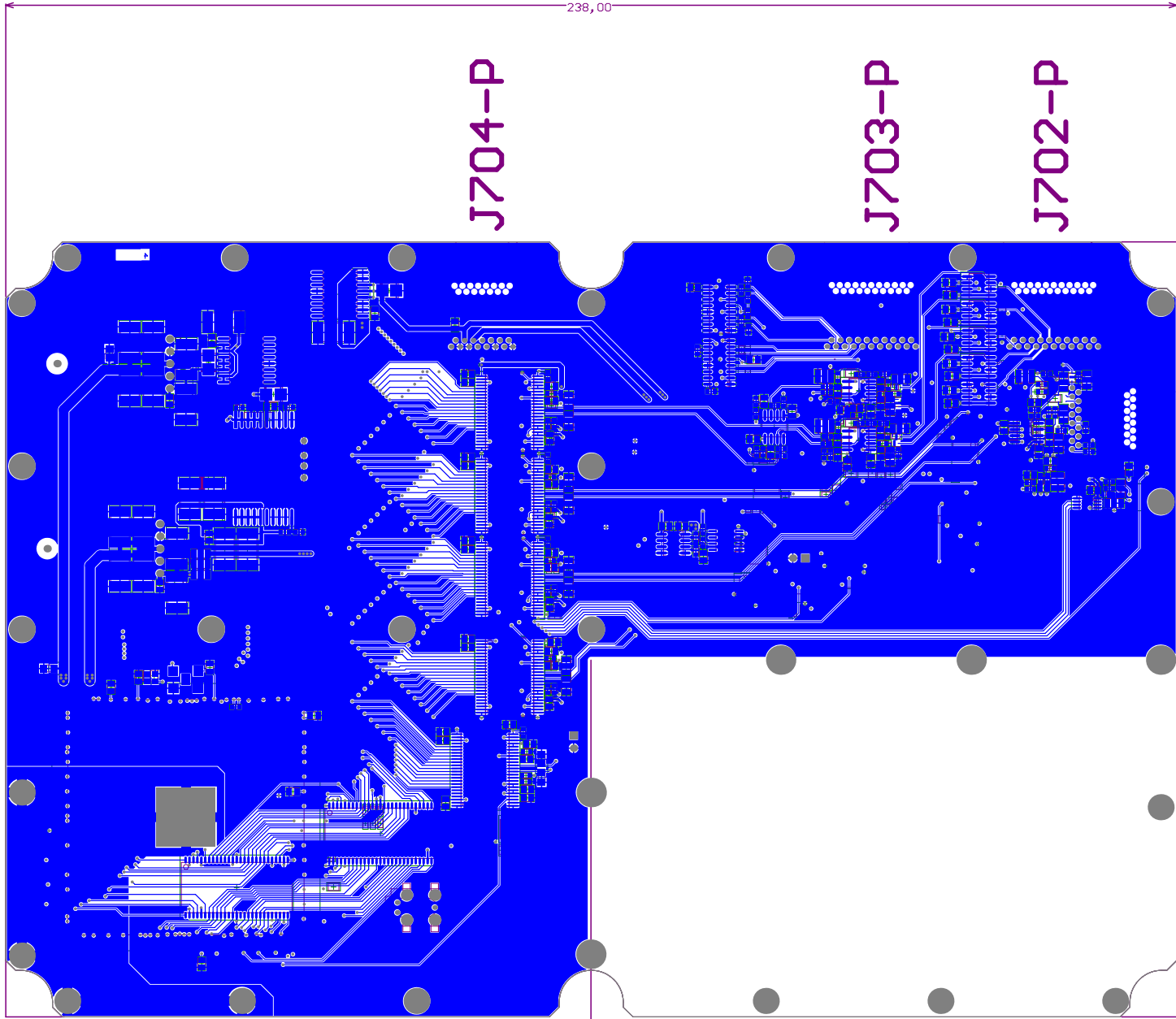




J701-P
B_LF/MF



158,00



238,00

J704-P

J703-P

J702-P

J701-P
B_LF/MF

158,00



238,00

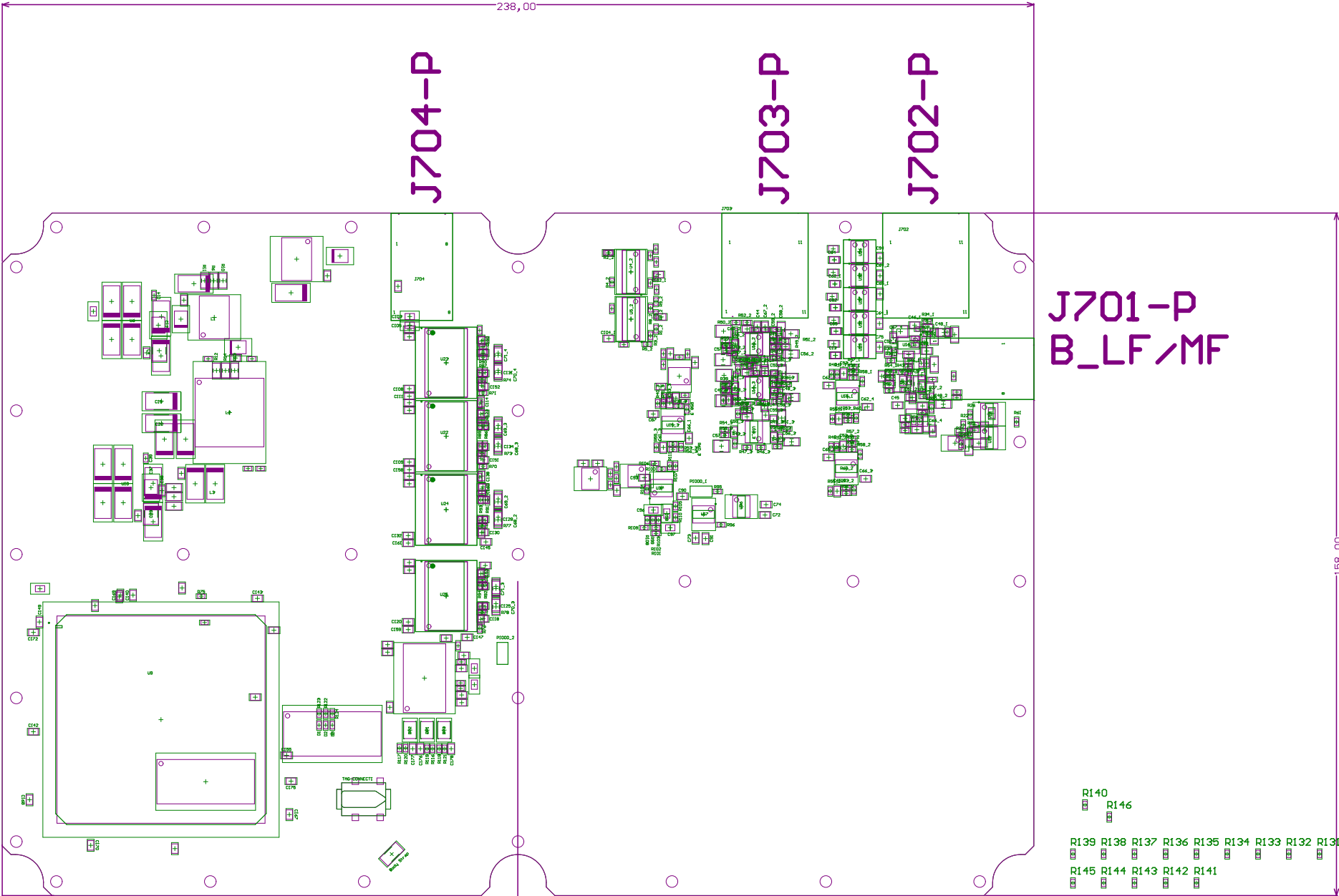
J704-P

J703-P

J702-P

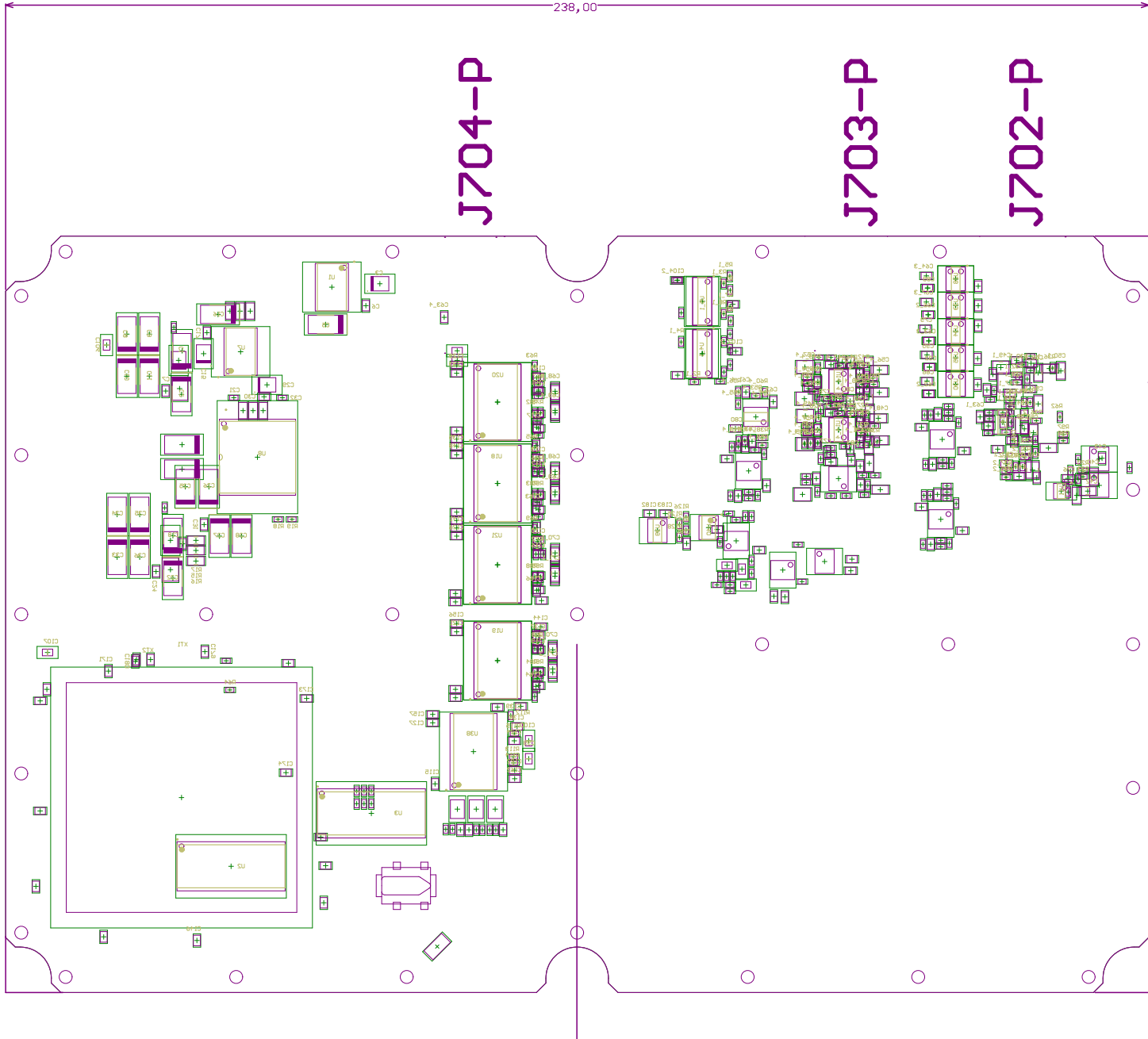
J701-P
B_LF/MF

158,00



R140
 R146

R139 R138 R137 R136 R135 R134 R133 R132 R131 R130 R129 R48 R44 R33 R29
 R145 R144 R143 R142 R141

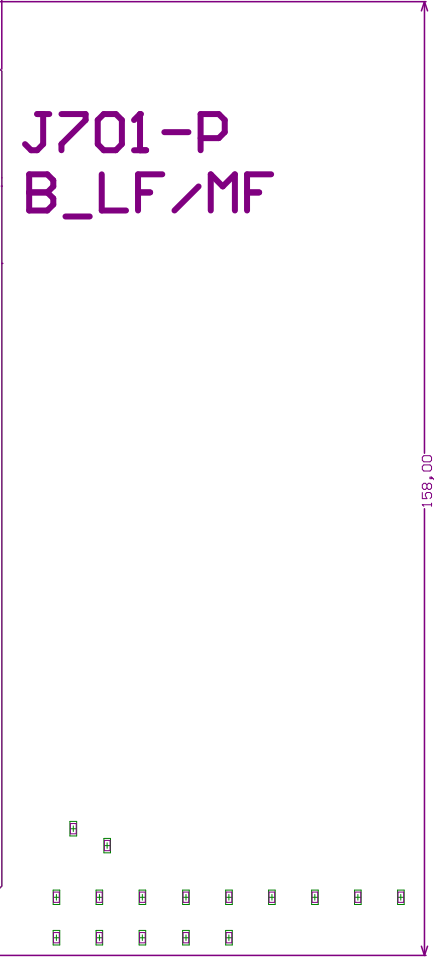


J704-P

J703-P

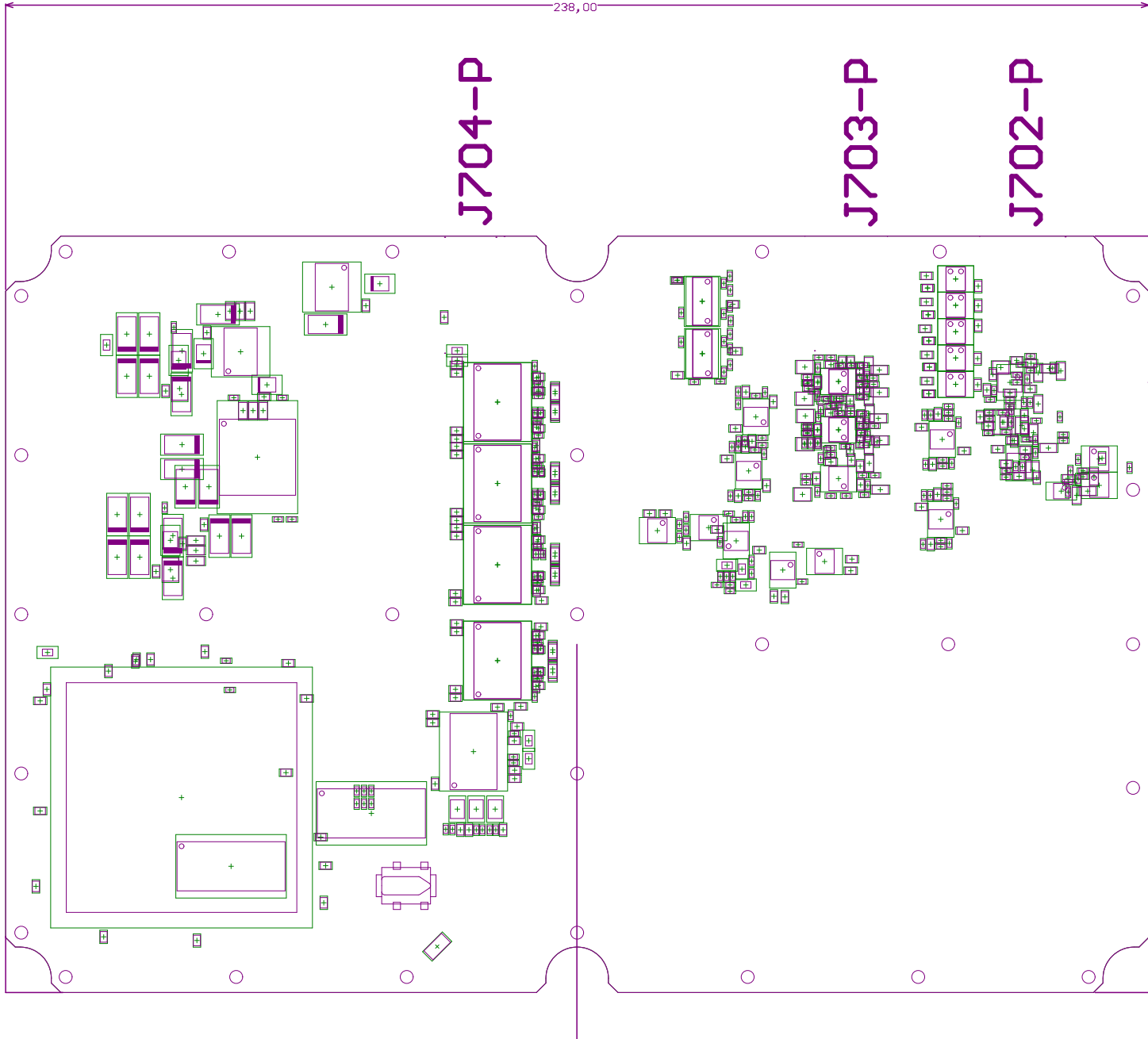
J702-P

238,00



J701-P
B_LF/MF

158,00

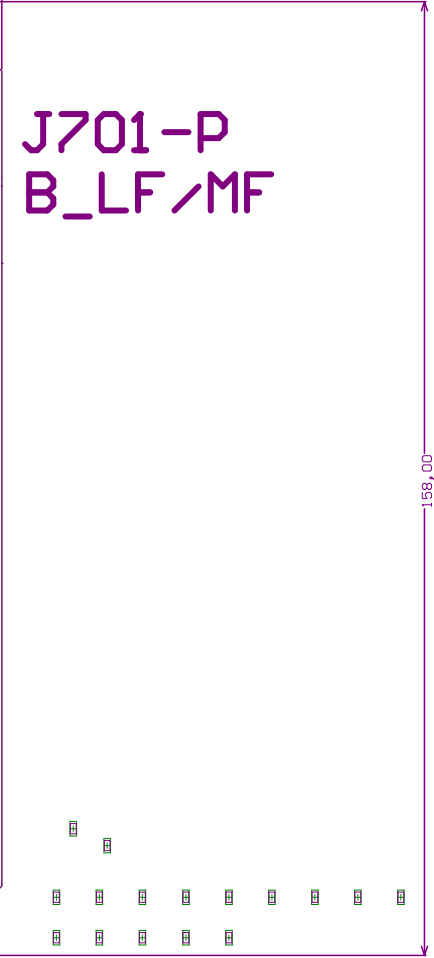


J704-P

J703-P

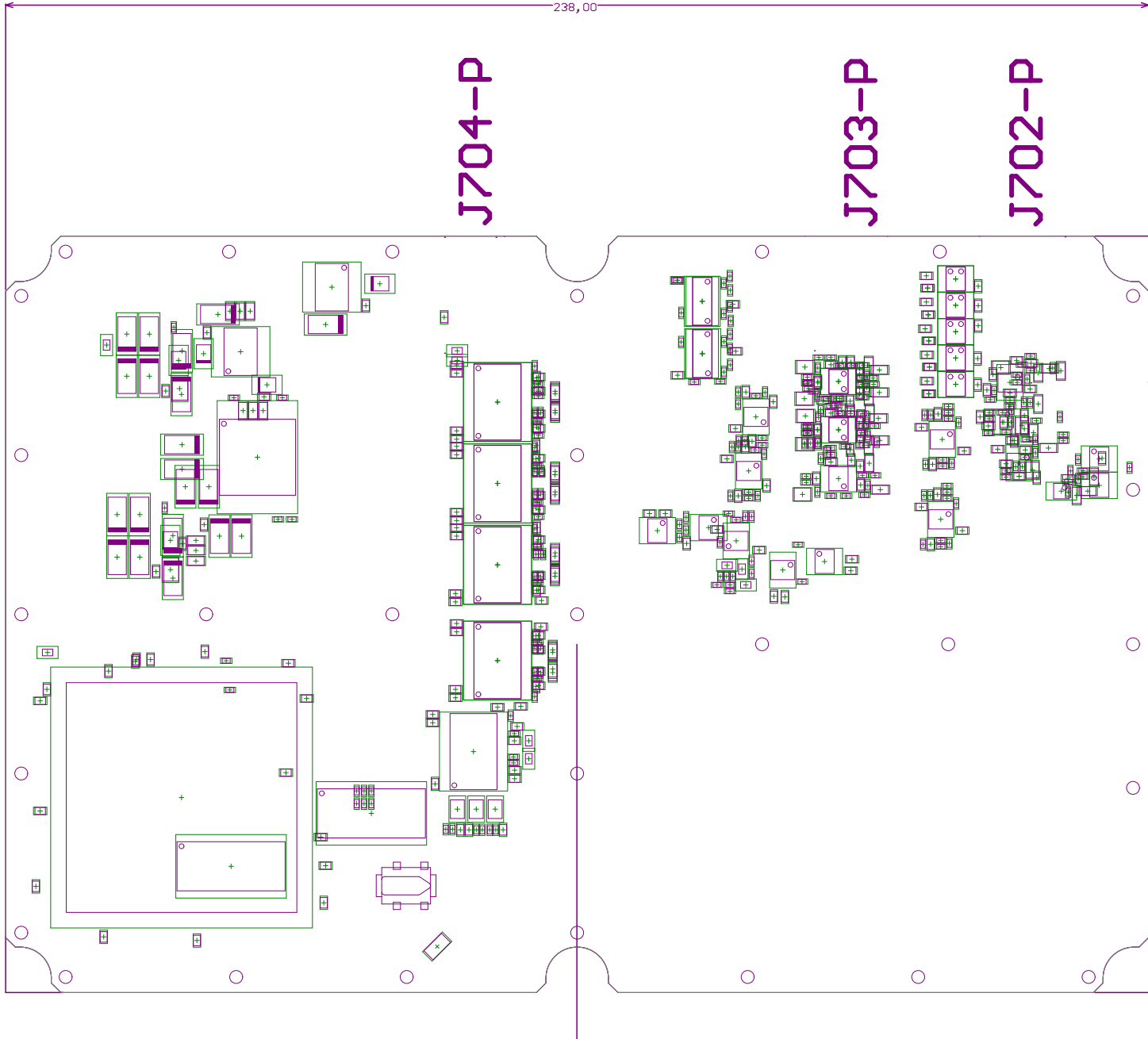
J702-P

238,00



J701-P
B_LF/MF

158,00



J704-P

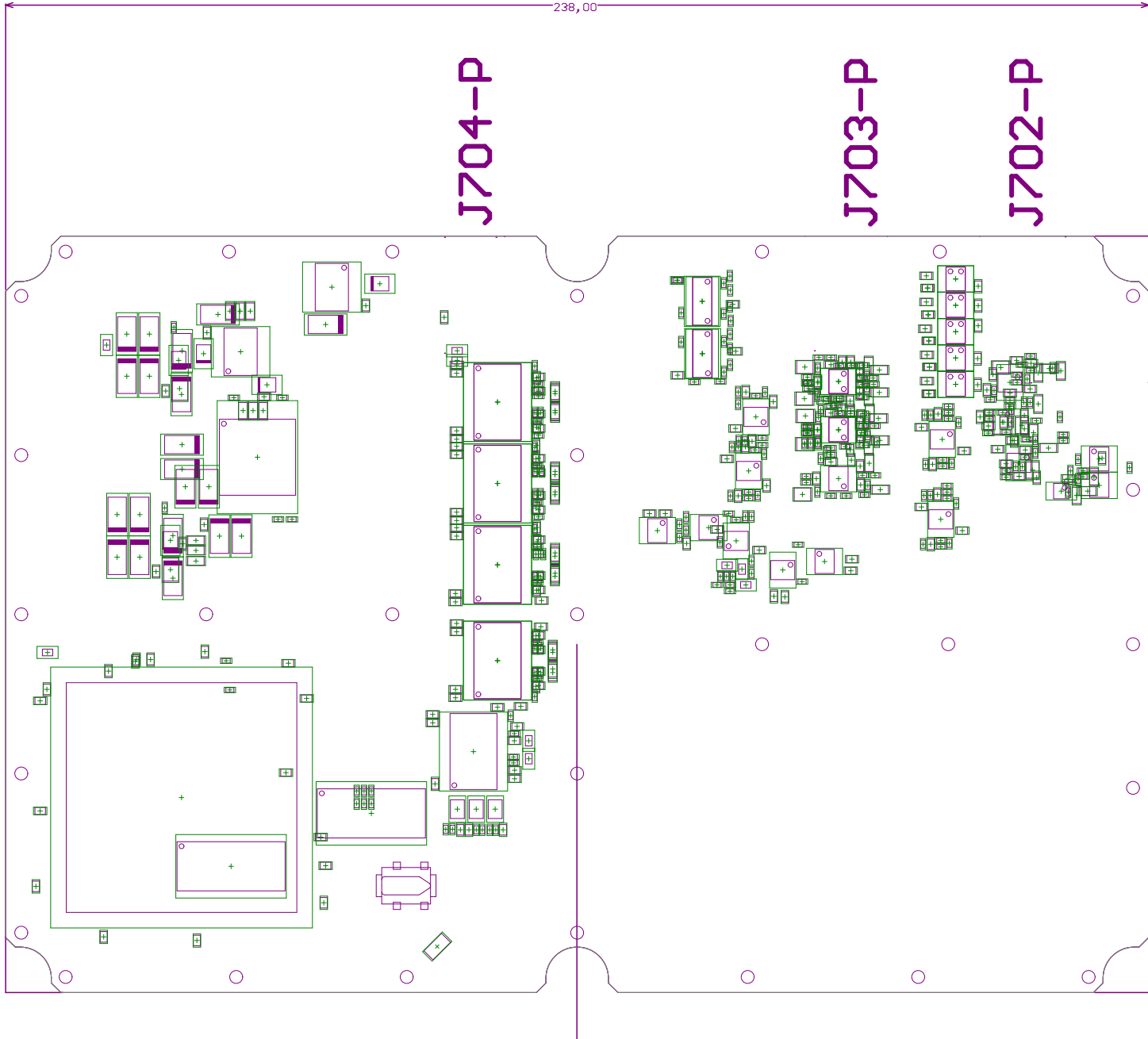
J703-P

J702-P

J701-P
B_LF/MF

158,00

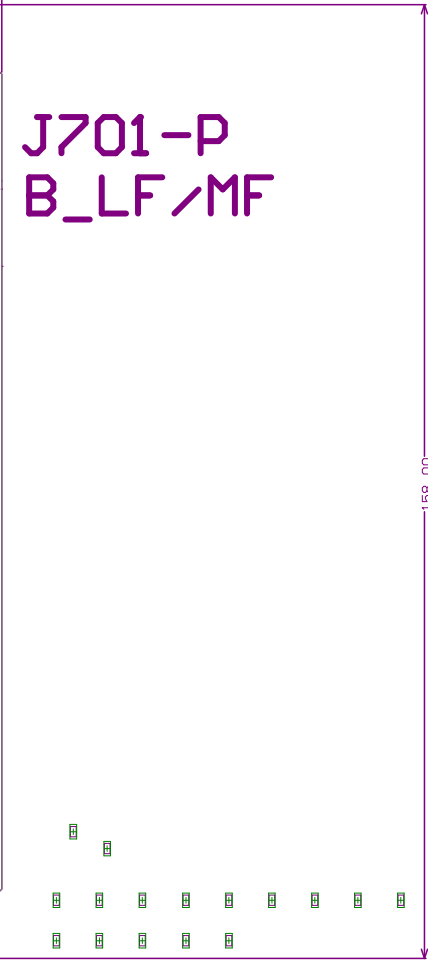
238,00



J704-P

J703-P

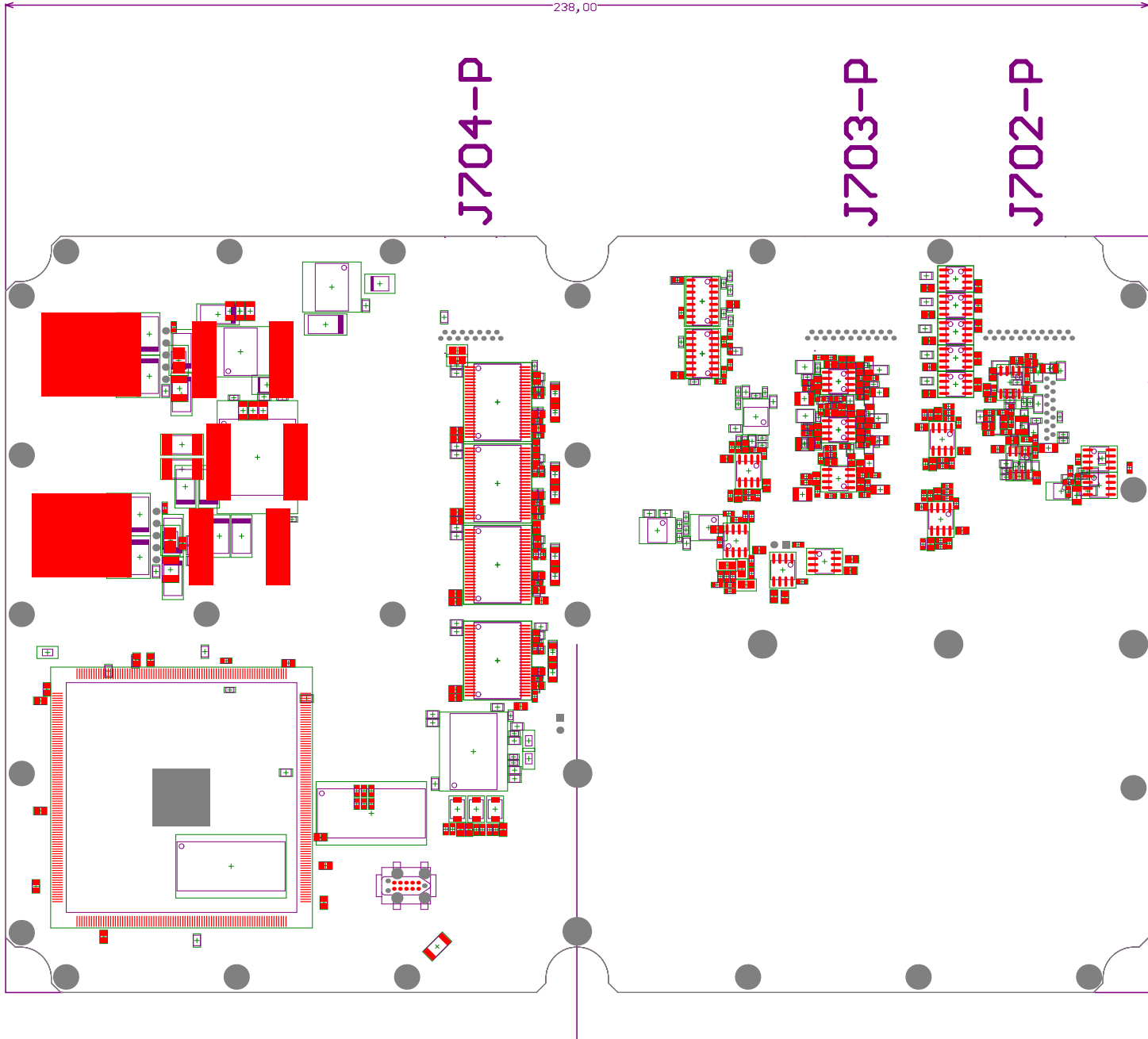
J702-P



J701-P
B_LF/MF

158,00

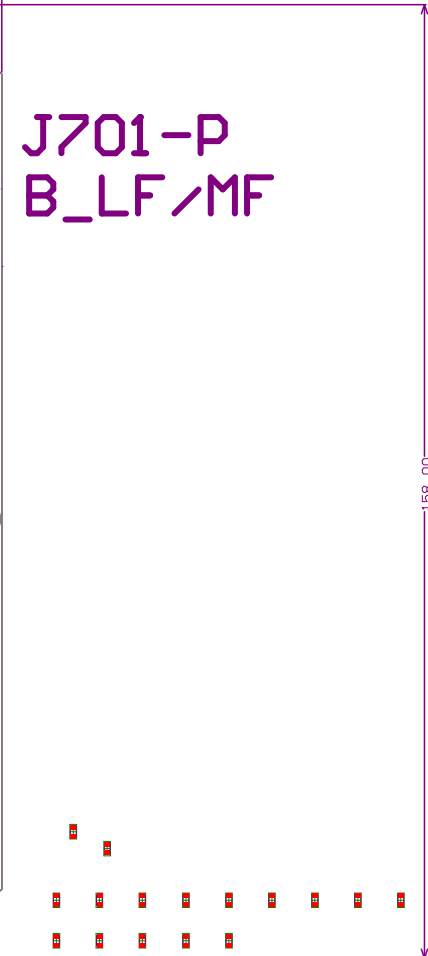
238,00



J704-P

J703-P

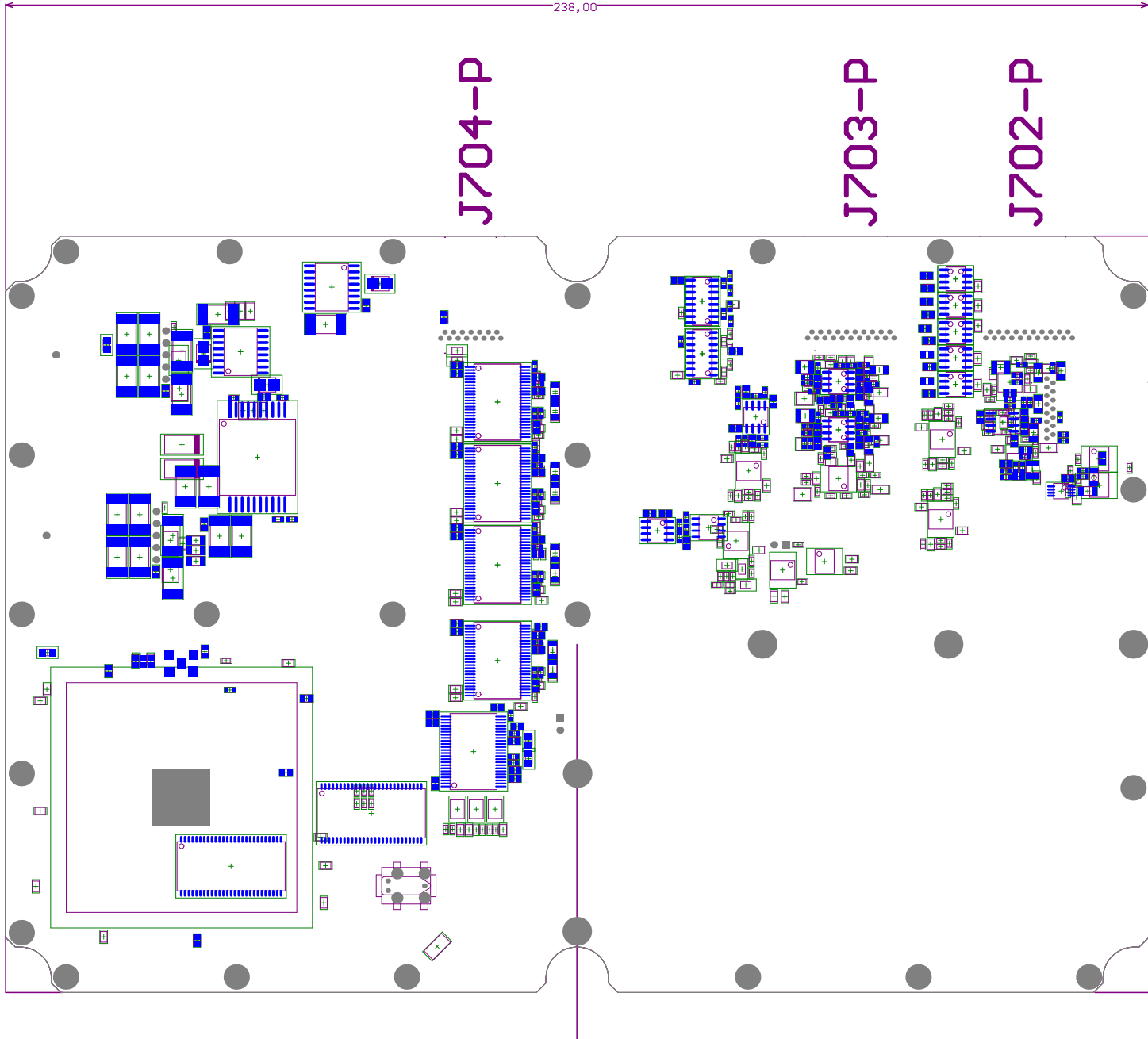
J702-P



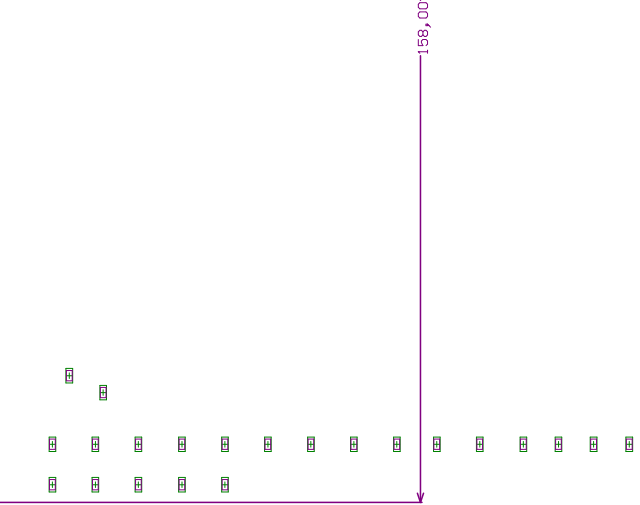
J701-P
B_LF/MF

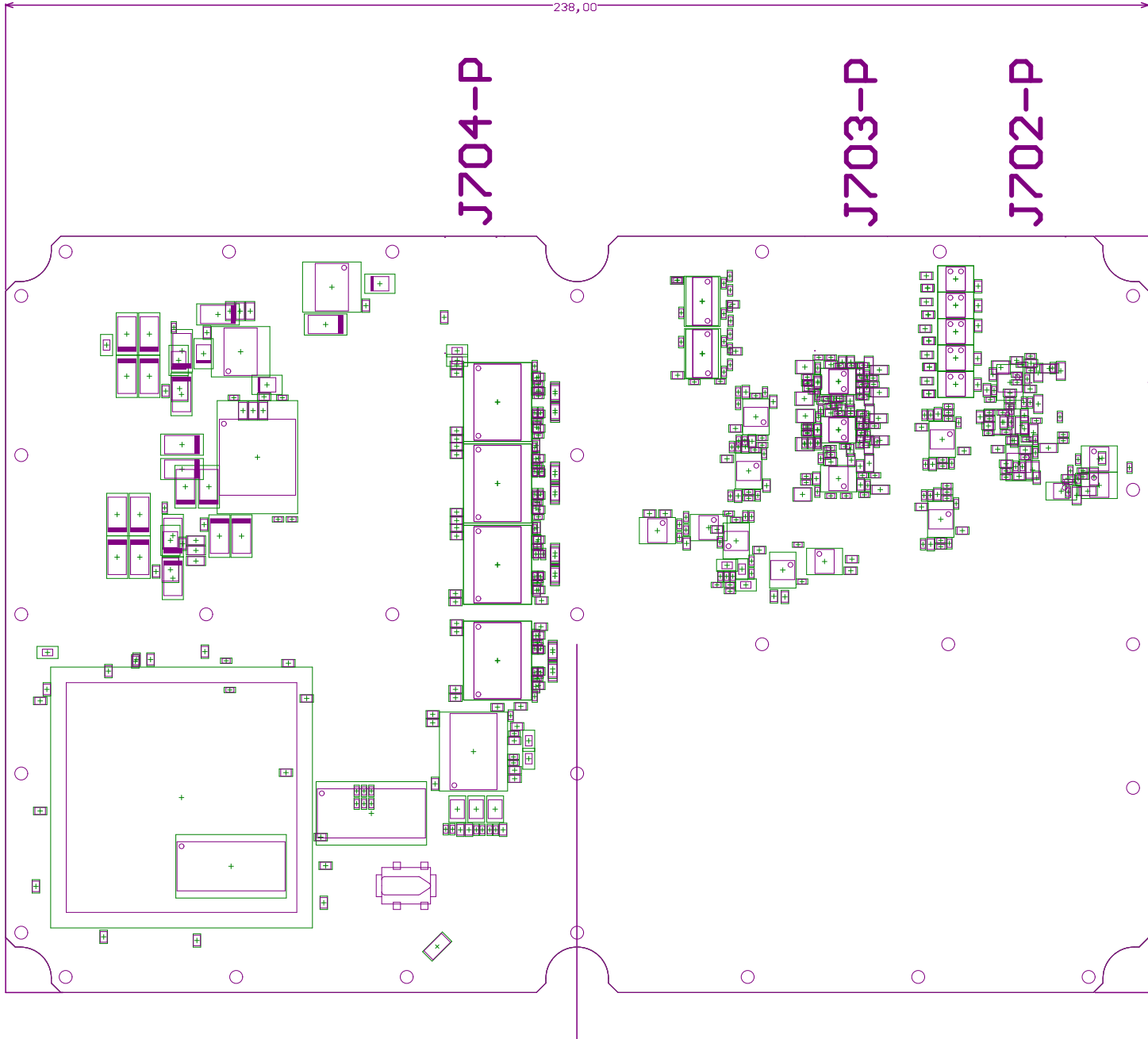
158,00

238,00



J701-P
B_LF/MF





J704-P

J703-P

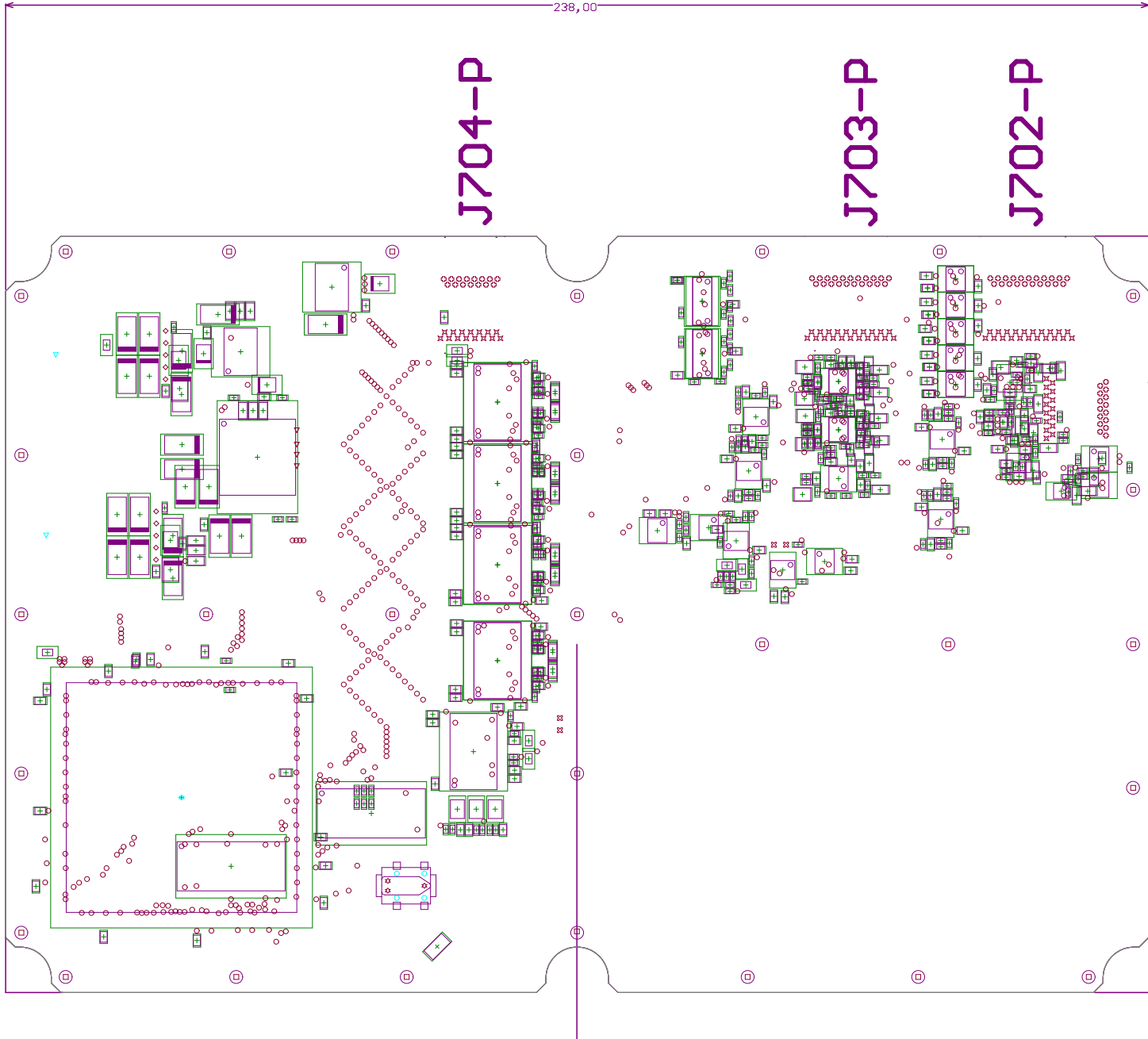
J702-P

238,00

J701-P
B_LF/MF

158,00





J704-P

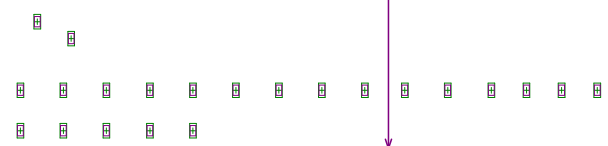
J703-P

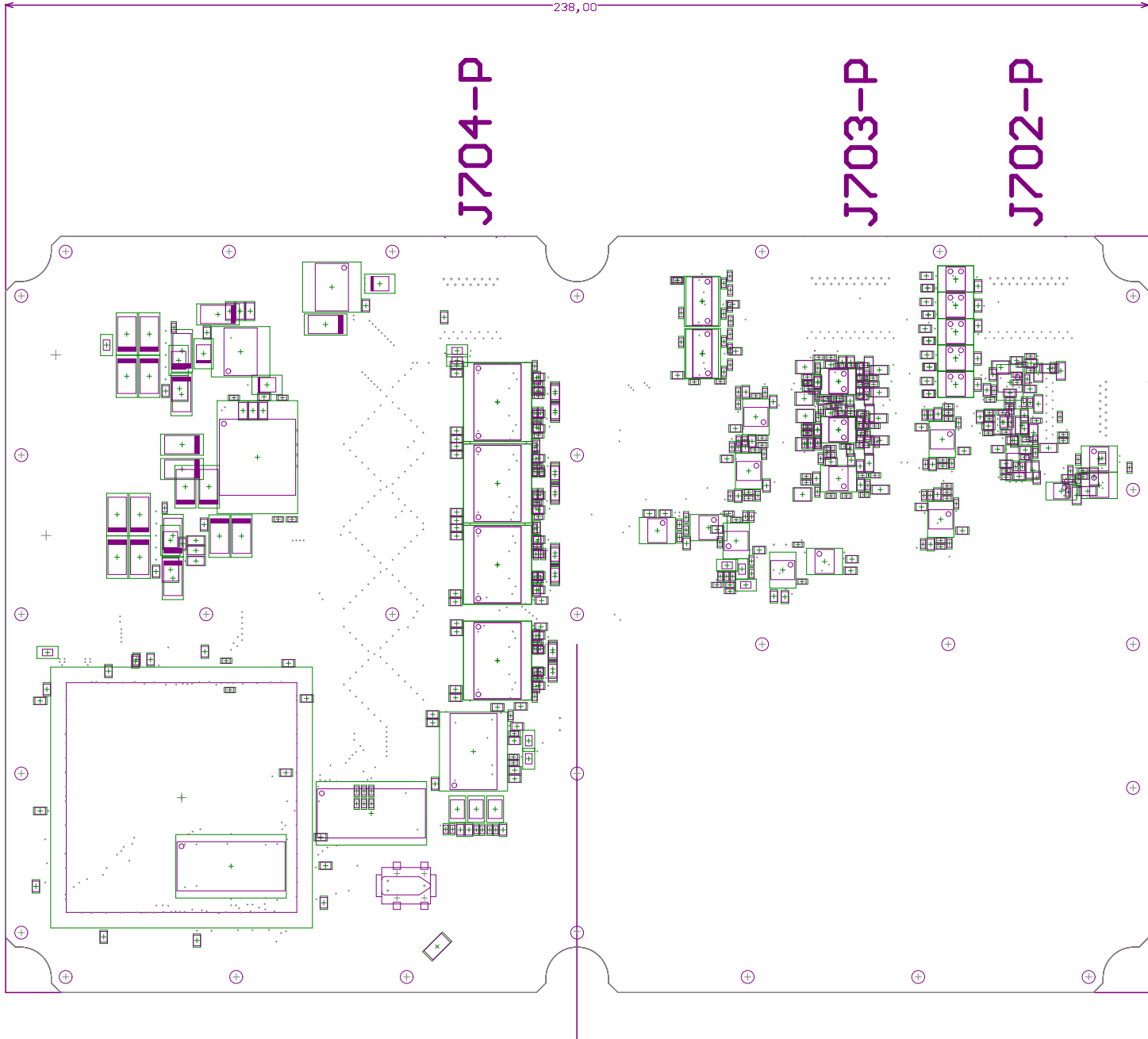
J702-P

238,00

J701-P
B_LF/MF

158,00



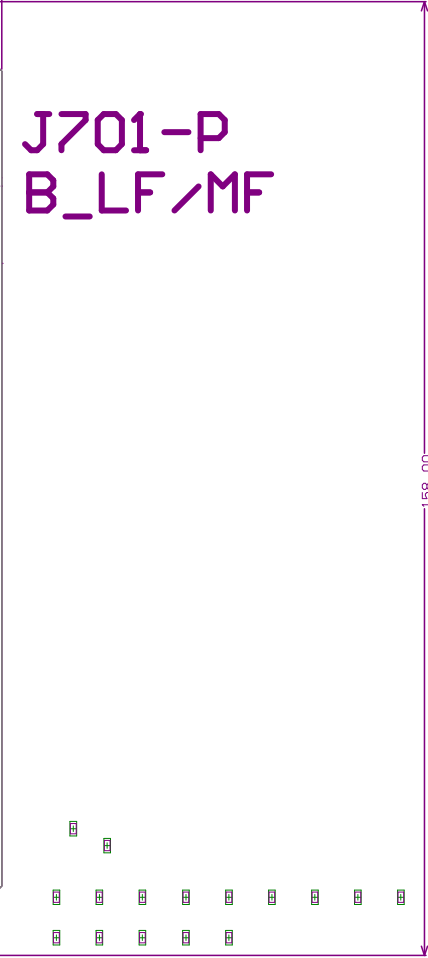


J704-P

J703-P

J702-P

238,00



J701-P
B_LF/MF

158,00



